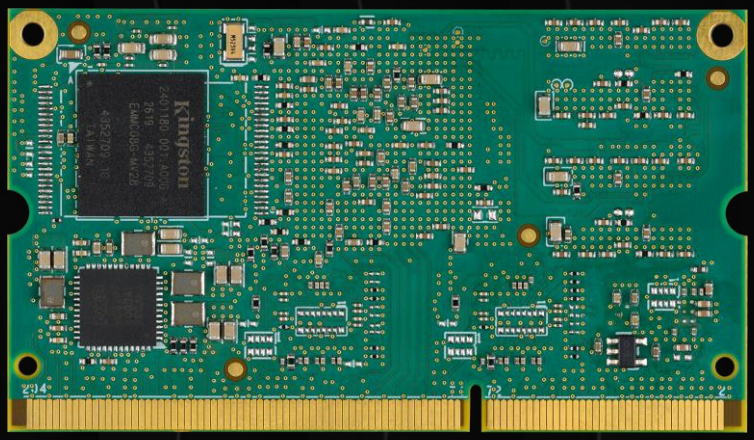
Rev. 1.02, 07/2026

VARISCITE LTD.

VAR-SOM-MX7-5G_V2

Datasheet

NXP/Freescale i.MX7™ - based System on Module



VARISCITE LTD.

VAR-SOM-MX7-5G_V2 Datasheet

© 2026 Variscite Ltd.
All Rights Reserved. No part of this document may be photocopied, reproduced, stored in a retrieval system, or transmitted, in any form or by any means whether, electronic, mechanical, or otherwise without the prior written permission of Variscite Ltd.
No warranty of accuracy is given concerning the contents of the information contained in this publication. To the extent permitted by law no liability (including liability to any person by reason of negligence) will be accepted by Variscite Ltd., its subsidiaries or employees for any direct or indirect loss or damage caused by omissions from or inaccuracies in this document. Variscite Ltd. reserves the right to change details in this publication without notice. Product and company names herein may be the trademarks of their respective owners.

Variscite Ltd.
4, Hamelacha Street
Lod
P.O.B 1121
Airport City, 70100
ISRAEL

Tel: +972 (9) 9562910
Fax: +972 (9) 9589477

Document Revision History

Revision	Date	Notes
1.00 (based on v2.6 for VAR-SOM-MX7-V1)	30/06/2026	Updated Wi-Fi + BT Section 2.4: Replaced LSR 450-0162R (Sterling-LWB5™) with Murata LPES5PL2DL Module (IW611 NXP Chipset). Updated 10/100/1000 Mbps Ethernet Transceiver Section 2.6: Replaced Atheros AR8033 & ADIN1300 with TI DP83867IRRGZ. Updated Section 7 to include a new mechanical drawing and an additional note on torque specifications.
1.01	01/07/2026	Updated Section 5.24: JTAG: TP locations were changed in V2 SOM. The image was updated accordingly.
1.02	12/07/2026	Updated Section 6.3: Power Consumption: Included measurements for the SoM's 3V3_RUN rail under active iPerf network load over 802.11n (2.4GHz) and 802.11ac (5GHz) Wi-Fi connections.

Document Revision History 3

1. Overview 6

1.1. General Information 6
1.2. Feature Summary 7
1.3. Block Diagram 8

2. Main Hardware Components 9

2.1. NXP i.MX7 9
2.2. Memory 13
2.3. WL8731L Audio 13
2.4. Wi-Fi + BT 14
2.5. PMIC 15
2.6. 10/100/1000 Mbps Ethernet Transceiver 16

3. External Connectors 17

3.1. VAR-SOM-MX7-5G_V2 Connector Pin-out 18
3.2. Pin Mux 24

4. SOM's interfaces 30

4.1. Display Interfaces 30
4.2. Camera Interfaces 35
4.3. Resistive Touch 38
4.4. Analog to Digital Converter 38
4.5. Gigabit Ethernet 39
4.6. 10/100/1000-Mbps Ethernet MAC (ENET) 40
4.7. Wi-Fi & Bluetooth 41
4.8. USB Ports 43
4.9. MMC/SD/SDIO 43
4.10. Audio 45
4.11. PCIe 47
4.12. Flexible Controller Area Network (FLEXCAN) 47
4.13. UART Interfaces 48
4.14. Enhanced Configurable SPI (ECSPI) 50
4.15. Quad Serial Peripheral Interface (QuadSPI) 52
4.16. I^2C 53
4.17. Subscriber Identification Module (SIM) 54
4.18. External Interface Module (EIM) 55
4.19. Pulse Width Modulation (PWM) 56
4.20. Keypad Port (KPP) 57
4.21. Flextimer (FTM) 57
4.22. Reference Clock Outputs/Inputs 58
4.23. General Purpose Input/Output (GPIO) 59
4.24. JTAG 62
4.25. General System Control 63
4.26. Power 64

5. Electrical specifications 65

5.1. Absolute maximum ratings 65
5.2. Operating conditions 65
5.3. Power Consumption 65

6. Environmental Specifications 66

7. Mechanical Drawings 67
8. Sticker 68
9. Legal Notice 69
10. Warranty Terms 70
11. Contact Information 71

1. Overview

1.1. General Information

The VAR-SOM-MX7-5G_V2 is a high-performance processing for low-power System-on-Module that perfectly fits various embedded products and the growing market of connected and portable devices and segment. It is based on the NXP/Freescale i.MX7 Dual family of multipurpose processors from which feature an ARM® Cortex™-A7 up to 1GHz + an additional ARM Cortex-M4.
This Heterogeneous Multicore Processing architecture enables the device to run an open operating system like Linux on the Cortex-A7 core and an RTOS like FreeRTOS™ on the Cortex-M4 core for time and security critical tasks.

The VAR-SOM-MX7-5G_V2 provides an ideal building block for simple integration with a wide range of products in target markets requiring high-performance processing with low power consumption, compact size and a very cost effective solution.

Supporting products:

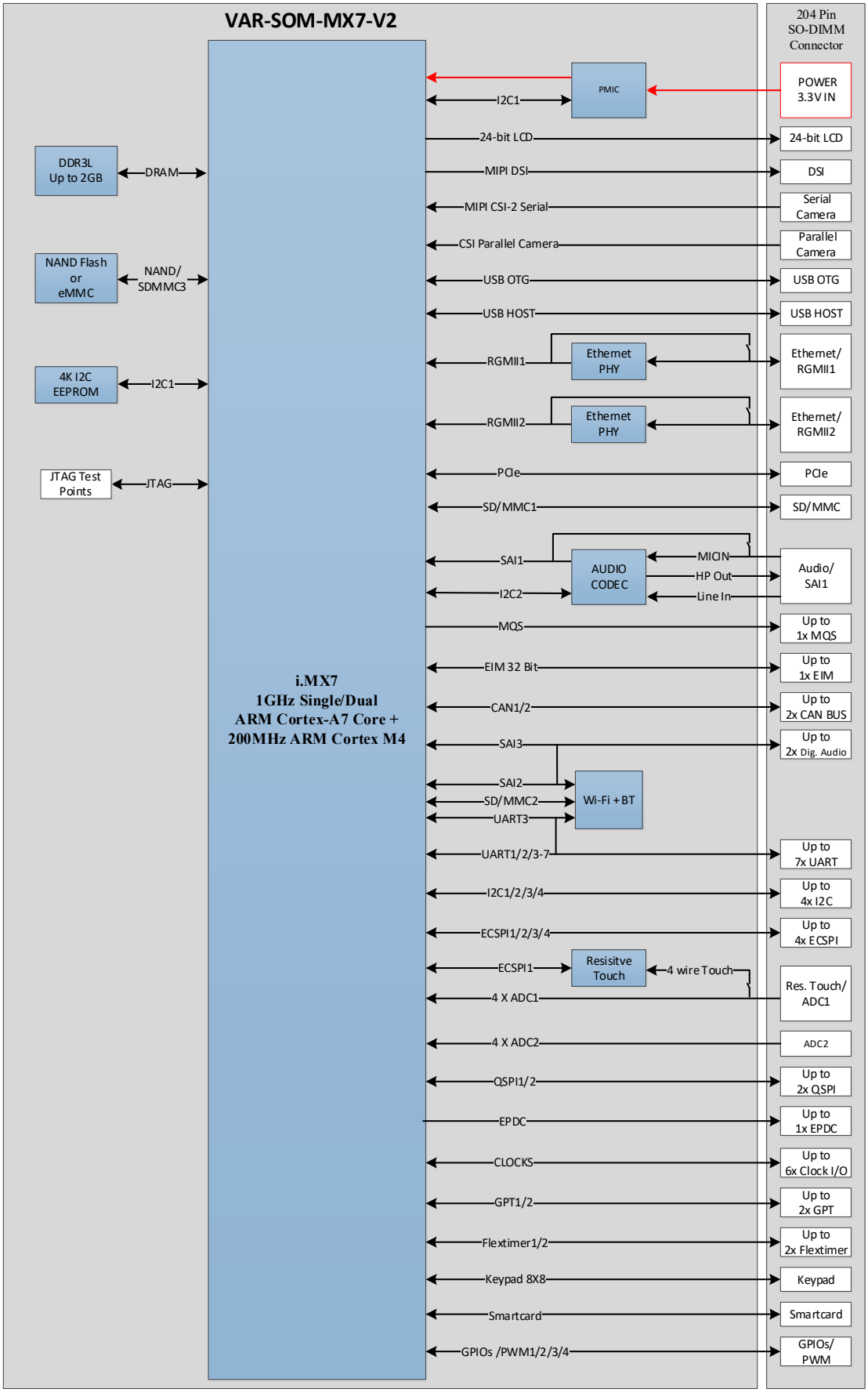
- VAR-MX7CustomBoard– evaluation board
  - ✓ Carrier -Board, compatible with VAR-SOM-MX7-5G_V2
  - ✓ Schematics
- VAR-DVK-MX7: full development kit, including:
  - ✓ VAR-MX7CustomBoard
  - ✓ VAR-SOM-MX7-5G_V2
  - ✓ Display and touch
  - ✓ Accessories and cables
- O.S support
  - ✓ Linux BSP

Contact Variscite support services for further information: mailto:support@variscite.com.

1.2. Feature Summary

- NXP/Freescale i.MX7 series SoC (Dual ARM® Cortex™-A7 Core, 1GHz/800Mhz + ARM® Cortex™-M4, 200MHz)
- Up to 2GB LPDDR2 RAM
- 8-bit NAND Flash Up 1GB or 128GB eMMC boot and storage
- 24 bit Parallel LCD interface
- Up to 1 x EPDC – Electrophoretic Display Controller interface
- 1 x MIPI DSI
- Parallel & serial camera interface
- Certified Wi-Fi 802.11 ac/a/b/g/n/ax (VAR-SOM-MX7-5G_V2)
- Bluetooth: 5.2/BLE
- Stereo line-In / headphones out
- Analog microphone
- 1 x USB 2.0 OTG
- 1 x USB 2.0 Host
- 1 x USB 2.0 HSIC Host
- Single /Dual 10/100/1000 Mbit/s Ethernet RGMII Interface
- 1 x SD/MMC
- PCIe v2.1
- 4-wire Resistive Touch
- Serial interfaces (ECSPI, QSPI, I2C, UART, SAI, MQS, JTAG)
- Up to 2 x ADC
- Up to 2 x CAN Bus
- Up to 1 x 32-bit EIM
- Up to 1 x (8 x8) Keypad interface
- Up to 1 x Smartcard interface
- Single power supply 3.3V
- SO-DIMM 204 Pin Connector

1.3. Block Diagram



2. Main Hardware Components

This section summarizes the main hardware building blocks of the VAR-SOM-MX7-5G_V2

2.1. NXP i.MX7

2.1.1. Overview

The i.MX7 family of processors represents NXP/Freescale's latest achievement in High-performance processing for low-power requirements with a high degree of functional integration. These processors are targeted towards the growing market of connected and Portable devices. The i.MX 7Dual family of processors features advanced implementation of the ARM® Cortex®-A7 core, which operates at speeds of up to 1 GHz. The i.MX 7Dual family provides up to 32-bit DDR3/DDR3L/LPDDR2/LPDDR3-1066 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth, GPS, displays, and camera sensors.

2.1.2. i.MX7D Block Diagram

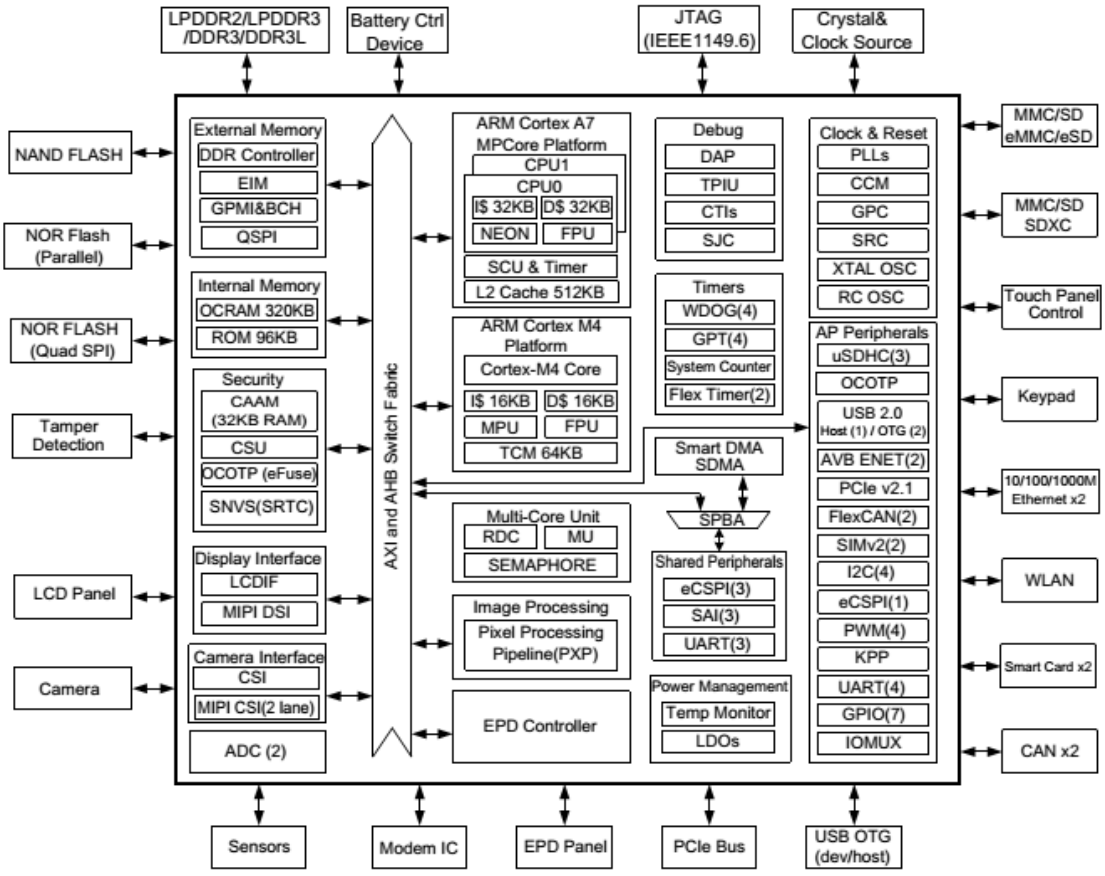


Figure 2. i.MX 7Dual System block diagram

2.1.3. CPU Platform

The i.MX7 Dual processor is based on ARM Cortex-A7 MPCore™ Platform and and an additional Cortex-M4 Core Platform.

The ARM Cortex-A7 MPCore™ Platform has the following features:

- Two/One ARM Cortex-A7 Cores (with TrustZone® technology) Symmetric CPU configuration where each CPU includes:
  - 32 Kbyte L1 Instruction Cache
  - 32 Kbyte L1 Data Cache
  - Private Timer and Watchdog
  - NEON MPE (media processing engine) coprocessor
- The ARM Cortex-A7 Core complex shares:
- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 512 KB unified I/D L2 cache
- Two master AXI bus interfaces output of L2 cache
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The ARM Cortex-M4 platform includes the following features:

- Cortex-M4 CPU core operating at 200 MHz
- MPU (memory protection unit)
- FPU (floating-point unit)
- 16 KByte instruction cache
- 16 KByte data cache
- 64 KByte TCM (tightly-coupled memory)

2.1.4. Memory Interfaces

The SoC-level memory system consists of the following components:

- Level 1 Cache - 32KB Instruction, 32KB Data cache
- Level 2 Cache - Unified instruction and data, 512KB
- On-Chip Memory:
  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 128KB)
  - Secure/nonsecure RAM (32 KB)
- External memory interfaces:
  - Up to 32-bit LP-DDR2-1066, DDR3-1066, DDR3L-1066, and LPDDR3-1066
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size,
    BA-NAND, PBA-NAND, LBA-NAND, OneNAND™and others. BCH ECC up to 62 bits.

- 16/32-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.

2.1.5. DMA engine

The SDMA is a multichannel flexible DMA engine. It helps in maximizing system performance by offloading the various cores in dynamic data routing. It has the following features:

- Powered by a 16-bit Instruction-Set micro-RISC engine
- Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels
- 48 events with total flexibility to trigger any combination of channels
- Memory accesses including linear, FIFO, and 2D addressing
- Shared peripherals between ARM and SDMA
- Very fast Context-Switching with 2-level priority based pre-emptive multi-tasking
- DMA units with auto-flush and prefetch capability
- Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address)
- DMA ports can handle unidirectional and bidirectional flows (Copy mode)
- Up to 8-word buffer for configurable burst transfers for EMIv2.5
- Support of byte-swapping and CRC calculations
- Library of Scripts and API is available

2.1.6. Image/Graphic Accelerators

The i.MX 7Dual makes use of dedicated HW image processing, in order to meet the targeted multimedia performance. The use of HW accelerators enables high performance at low power dissipation and lowers the CPU utilization, allowing it to be used for other tasks.

The i.MX7 Dual incorporate the following graphical hardware accelerators:

- ePXP – Enhanced PiXel Processing engine to offloading key pixel processing
- operations required to support both LCD and EPD display applications
    - EPD display support including collision detection and auto-waveform selection
    - Multiple input/output format support, including YUV / RGB / Gray Scale
    - Support both RGB/YUV scaling
    - Support overlay with Alpha blending
    - RGB656/RGB444 to RGBW4444 conversion with LUT for color EPD panel
    - Color space conversion (CSC) , secondary color space conversion (CSC2), and rotation

2.1.7. Display and Camera Interfaces

i.MX7 has both parallel LCD interface and EPD panel interface (i.MX7 Dual only) to support eReaders with either LCD panel or EPD panel, or both of them

- EPDC – Supporting direct-driver for E-Ink EPD panels with up to 2048 x 1536 at 106 Hz refresh (or 4096 x 4096 at 20 Hz)
    - Support up to 64 LUT for concurrent update

- Support Auto-Waveform selection based on both input image and current panel content
- Support collision detection

- LCDIF supporting one parallel 24-bit LCD display with resolution up to 1920x1080 at 60Hz
- MIPI DSI host controller and D-PHY:
  - Supports 2 data lanes and 1 clock lane
  - Maximum bit rate of 1.5 Gbps
- CMOS sensor interface (CSI) supporting up to one parallel 24-bit camera interface
- MIPI CSI-2 controller and D-PHY:
  - Supports 2 data lanes and 1 clock lane
  - Maximum bit rate of 1.5 Gbps

2.1.8. Audio Back End

The Audio subsystem includes the following:

- Three synchronous audio interface (SAI) modules supporting s full-duplex serial interfaces with frame synchronization such as I2S, AC97, TDM, and codec/DSP interfaces.
- Medium Quality Sound (MQS) for low-cost stereo audio output

2.1.9. 10/100/1000 Ethernet Controller

The MAC-NET core, in conjunction with a 10/100/1000 MAC, implements layer 3 network acceleration functions. These functions are designed to accelerate the processing of various common networking protocols, such as IP, TCP, UDP and ICMP, providing wire speed services to client applications.

The core implements a triple-speed 10/100/1000-Mbit/s Ethernet MAC compliant with the IEEE802.3-2002 standard. The MAC layer provides compatibility with half- or full duplex 10/100-Mbit/s and full-duplex gigabit Ethernet LANs.

The MAC operation is fully programmable and can be used in Network Interface Card (NIC), bridging, or switching applications. The core implements the remote network monitoring (RMON) counters according to IETF RFC 2819.

The core also implements a hardware acceleration block to optimize the performance of network controllers providing TCP/IP, UDP, and ICMP protocol services. The acceleration block performs critical functions in hardware, which are typically implemented with large software overhead.

The core implements programmable embedded FIFOs that can provide buffering on the receive path for lossless flow control.

Advanced power management features are available with magic packet detection and programmable power-down modes.

A unified DMA (uDMA), internal to the ENET module, optimizes data transfer between the ENET core and the SoC, and supports an enhanced buffer descriptor programming model to support IEEE 1588 functionality.

The programmable Ethernet MAC with IEEE 1588 integrates a standard IEEE 802.3 Ethernet MAC with a time-stamping module. The IEEE 1588 standard provides accurate clock synchronization for distributed control nodes for industrial automation applications.

2.2. Memory

2.2.1. RAM

The VAR-SOM-MX7-5G_V2 is available with up to 2 GB of DDR3L memory.

2.2.2. Non-volatile Storage Memory

The VAR-SOM-MX7-5G_V2 is available with a variety of non-volatile storage memory options, used for Flash Disk purposes, O.S. run-time-image, Boot-loader and application/user data storage.
The VAR-SOM-MX7-5G_V2 can arrive with up to 1GB SLC NAND flash or up to 128GB MLC eMMC

Note:
[1] eMMC is available only on iMX7D based SOMs.
[2] It is not possible to use both on-SOM NAND and eMMC at the same time.

2.3. WL8731L Audio

The WM8731L is low power stereo CODEC with an integrated headphone driver. The WM8731/L is designed specifically for portable MP3 audio and speech players and recorders. The WM8731 is also ideal for MD, CD-RW machines and DAT recorders. Stereo line and mono microphone level audio inputs are provided, along with a mute function, programmable line level volume control and a bias voltage output suitable for an electret type microphone. Stereo 24-bit multi-bit sigma delta ADCs and DACs are used with oversampling digital interpolation and decimation filters. Digital audio input word lengths from 16-32 bits and sampling rates from 8kHz to 96kHz are supported. Stereo audio outputs are buffered for driving headphones from a programmable volume control, line level outputs are also provided along with anti-thump mute and power up/down circuitry.
Features:

- Highly Efficient Headphone Driver
- Audio Performance
  - ✓ ADC SNR 90dB ('A' weighted)
  - ✓ DAC SNR 100dB ('A' weighted)
- ADC and DAC Sampling Frequency: 8kHz – 96kHz
- Selectable ADC High Pass Filter
- 2 or 3-Wire MPU Serial Control Interface
- Programmable Audio Data Interface Modes
  - ✓ I2S, Left, Right Justified or DSP
  - ✓ 16/20/24/32 bit Word Lengths
  - ✓ Master or Slave Clocking Mode
- Microphone Input and Electret Bias with Side Tone Mixer Digital microphone

2.4. Wi-Fi + BT

The VAR-SOM-MX7-5G_V2 contains a certified high-performance Wi-Fi, Bluetooth, 802.15.4 module:

- Wi-Fi® 802.11a/b/g/n/ac/ax
- Bluetooth® 5.4 BR/EDR/LE
- 802.15.4
- Modules have an antenna connection through a U. FL JACK connector
- Antenna cable connected to module must have 50-Ω impedance

Figure illustrates the VAR-SOM-MX8M-PLUS internal Wi-Fi and BT connectivity.

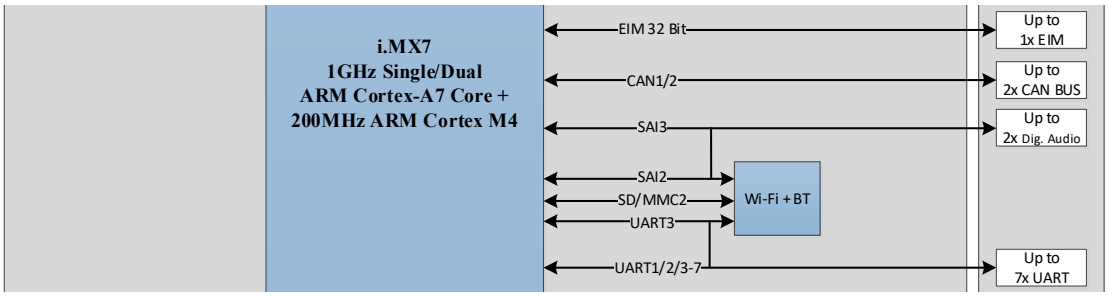


Figure 1: VAR-SOM-MX7-5G_V2 Wi-Fi & BT Internal Connection

2.4.1. Interface Implementation Options

2.4.1.1 Module Configuration with "WBD" Option

- System use**: Wi-Fi and Bluetooth**.
  - BT UART external interface pins should be left floating.
- System use: **Wi-Fi and no BT**.
  - In this case, disable the BT buffer (using GPIO1_IO[6]) and BT function.
  - BT UART interface pins can be used externally with any of the alternate functions.
- System use: **BT and no Wi-Fi.**
  - Disable Wi-Fi function.
  - Enable the BT buffer (using GPIO1_IO[6]) and BT function.

2.4.1.2 Module Configuration without "WBD" Option

  - BT UART interface accessible externally with any of its alternative functions.
  - uSDHC2: Routed directly to the designated Murata LPES5PL2DL Wi-Fi module footprint. These pins are left unconnected (floating) when the Wi-Fi module is not populated and they are not exported to the SODIMM connector.

2.4.2. Bluetooth Interface Signals

Table 20: BT UART Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
50		uart3.CTS_B	1	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.M06
51		uart3.RTS_B	1	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.M05
52		uart3.TX	1	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.M02
53		uart3.RX	1	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.M01

2.4.3. Wi-Fi Control Signals

3. ***Table 21: WIFI control Interface Signals***

Pin#	Assy	Pin Function	Alt#	Notes	Ball
82	WBRST	IND_RST_WL		Pin referenced to 1.8V	LBES5PL2xL.63
70	WBRST	IND_RST_BT		Pin referenced to 1.8V	LBES5PL2xL.64

3.1. PMIC

The VAR-SOM-MX7-5G_V2 features Freescale/NXP's PF3000 as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX7 series of application processors. The PMPF0100 regulates all power rails required on SoM from a single 3.3V power supply.
The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

3.2. 10/100/1000 Mbps Ethernet Transceiver

The SOM includes Texas Instruments DP83867IRRGZ Ethernet Transceiver
The DP83867IRRGZ device is a robust, low power, fully featured Physical Layer transceiver with integrated PMD sublayers to support 10BASE-Te, 100BASETX and 1000BASE-T Ethernet protocols.
The DP83867 is designed for easy implementation of 10/100/1000Mbps Ethernet LANs. DP83867 interfaces directly to twisted pair media via an external transformer. This device interfaces directly to the MAC layer through the IEEE 802.3 Reduced GMII (RGMII).

Key features include:

- Ultra low RGMII latency TX < 90ns, RX < 290ns
- Time Sensitive Network (TSN) compliant
- 16 programmable RGMII delay modes on RX/TX
- Integrated MDI termination resistors
- Programmable RGMII termination impedance
- WoL (Wake-on-LAN) packet detection
- Start of Frame Detect for IEEE 1588 time stamp
- RJ45 mirror mode
- Fully compatible to IEEE 802.3 10BASE-Te, 100BASE-TX, and 1000BASE-T Specification Cable diagnostics

4. External Connectors

The VAR-SOM-MX7-5G_V2 exposes a 204 pin SO-DIMM connector.
Recommended mating Connector socket for Customboard interfacing are the following connectors (or equivalent):

1. Cvilux CS69-2042CA0-R0
2. TE Connectivity 2-2013289-1
3. JAE MM80-204B1-1

Pin#:
Pin number on the connector

Signal:
Default VAR-SOM-MX7-5G_V2 Signal

Type:
Pin type & direction:

- I – In
- O – Out
- DS – Differential Signal
- A – Analog
- Power – Power Pin

Pin Description:
Pin functionality group

i.MX7 Ball:
Ball number

Mode (Tables 3.2 & 3.4):
Pin mux mode option

4.1. VAR-SOM-MX7-5G_V2 Connector Pin-out

Pin #	Signal	Type	Description	GPIO	Ball
1*	MICBIAS / GPIO1_IO[1] –No Codec	AO / IO	Audio Interface Microphone Bias / General Purpose Input Output Register 1 Bit 1	GPIO1_IO[1]	WM8731L.21 N02
2	LCD_DATA10	IO	LCD Interface Data 10		L24
3	MICIN	AI	Audio Interface Microphone In		WM8731L.22
4	LCD_ENABLE	IO	LCD Interface Data Enable	GPIO2_IO[1]	P21
5	AGND	POWER	Audio GND		WM8731L.19
6	LCD_DATA4	IO	LCD Interface Data 4	GPIO2_IO[4]	N22
7*	RLINEIN / GPIO7_IO[14] -No Codec	AI / IO	Audio Interface Line In Right / General Purpose Input Output Register 7 Bit 14	GPIO7_IO[14]	WM8731L.23 E19
8	LCD_DATA9	IO	LCD Interface Data 9	GPIO2_IO[9]	L25
9*	LLINEIN / GPIO7_IO[12] -No Codec	AI / IO	Audio Interface Line In Left / General Purpose Input Output Register 7 Bit 12	GPIO7_IO[12]	WM8731L.24 D16
10	LCD_DATA15	IO	LCD Interface Data 15	GPIO2_IO[15]	K25
11	AGND	POWER	Audio GND		
12	LCD_HSYNC	IO	LCD Interface Horizontal Sync	GPIO2_IO[3]	N21
13*	HPROUT / GPIO7_IO[13] -No Codec	AO / IO	Audio Interface Headphones Right Output / General Purpose Input Output Register 7 Bit 13	GPIO7_IO[13]	WM8731L.14 D15
14	LCD_VSYNC	IO	LCD Interface Vertical Sync	GPIO2_IO[2]	N20
15*	HPLOUT / GPIO7_IO[15] -No Codec	AO / IO	Audio Interface Headphones Left Output / General Purpose Input Output Register 7 Bit 15	GPIO7_IO[15]	WM8731L.13 D19
16	LCD_CLK	IO	LCD Interface Pixel Clock	GPIO2_IO[0]	P20
17	LCD_DATA8	IO	LCD Interface Data 8	GPIO2_IO[8]	M23
18	LCD_DATA11	IO	LCD Interface Data 11	GPIO2_IO[11]	L23
19	LCD_DATA7	IO	LCD Interface Data 7	GPIO2_IO[7]	M22
20	LCD_DATA22	IO	LCD Interface Data 22	GPIO3_IO[27]	D25
21	LCD_DATA6	IO	LCD Interface Data 6	(GPIO2_IO[6]	M21
22	LCD_DATA21	IO	LCD Interface Data 21	GPIO3_IO[26]	E24
23^	LCD_DATA1	IO	LCD Interface Data 1	GPIO3_IO[6]	A22
24	LCD_DATA14	IO	LCD Interface Data 14	GPIO2_IO[14]	L20
25	LCD_DATA12	IO	LCD Interface Data 12	GPIO2_IO[12]	L22
26	LCD_DATA23	IO	LCD Interface Data 23	GPIO3_IO[28]	G23
27^	LCD_DATA2	IO	LCD Interface Data 2	GPIO3_IO[7]	B22
28^	LCD_DATA19	IO	LCD Interface Data 19	GPIO3_IO[24]	D24
29^	LCD_DATA16	IO	LCD Interface Data 16	GPIO3_IO[21]	B25
30	LCD_DATA20	IO	LCD Interface Data 20	GPIO3_IO[25]	C25
31^	LCD_DATA3	IO	LCD Interface Data 3	GPIO3_IO[8]	A23
32	LCD_DATA5	IO	LCD Interface Data 5	GPIO2_IO[5]	M20
33^	LCD_DATA18	IO	LCD Interface Data 18	GPIO3_IO[23]	E23
34	LCD_DATA13	IO	LCD Interface Data 13	GPIO2_IO[13]	L21
35	TS_X+ / ADC1_IN3 -No TSC	AI / AI	Touch screen interface / Analog to Digital Converter 1 channel 3 (1.8V)		TSC2046.6 AE03
36	LCD_RESET	IO	LCD Interface Reset	GPIO3_IO[4]	C21
37	TS_Y+ / ADC1_IN1 -No TSC	AI / AI	Touch screen interface / Analog to Digital Converter 1 channel 1 (1.8V)		TSC2046.7 AD03
38^	LCD_DATA17	IO	LCD Interface Data 17	GPIO3_IO[22]	G21

Pin #	Signal	Type	Description	GPIO	Ball
39	TS_X- / ADC1_IN2 -No TSC	AI / AI	Touch screen interface / Analog to Digital Converter 1 channel 2 (1.8V)		TSC2046.8 AE02
40^	LCD_DATA0	IO	LCD Interface Data 0	GPIO3_IO[5]	D21
41	TS_Y- / ADC1_IN0 -No TSC	AI / AI	Touch screen interface / Analog to Digital Converter 1 channel 0 (1.8V)		TSC2046.9 AD01
42	UART2_TX	IO	UART 2 TX line	GPIO3_IO[1]	F25
43~	ETH_MDIO_DATA	IO	Ethernet Management Data IO Interface Data – Function Must not be Altered if Ethernet PHY is assembled	GPIO5_IO[9]	D03
44	UART2_RTS_B	IO	UART 2 RTS line	GPIO3_IO[2]	E25
45~	ETH_MDIO_CLK	IO	Ethernet Management Data IO Interface Clock – Function Must not be Altered if Ethernet PHY is assembled	GPIO5_IO[10]	C03
46	UART2_CTS_B	IO	UART 2 CTS line	GPIO3_IO[3]	F24
47	GND	POWER	Digital GND		
48	UART2_RX	IO	UART 2 RX line	GPIO3_IO[0]	E20
49*	ETH2_MDI_A_P / GPIO2_IO[16] -No ETH PHY2	DS / IO	Gigabit Ethernet2 Positive Lane A/ General Purpose Input Output Register 2 Bit 16	GPIO2_IO[16]	DP83867IR_2.1 J21
50^	CSI1_MCLK	IO	Parallel Camera Master clock	GPIO3_IO[12]	F20
51*	ETH2_MDI_A_M / GPIO2_IO[17] -No ETH PHY2	DS / IO	Gigabit Ethernet2 Negative Lane A/ General Purpose Input Output Register 2 Bit 17	GPIO2_IO[17]	DP83867IR_2.2 J20
52^	CSI1_DATA[9]	IO	Camera Sensor Data Bit 14	GPIO3_IO[13]	E21
53	GND	POWER	Digital GND		
54^	CSI1_DATA[6]	IO	Parallel Camera Data bit 6	GPIO3_IO[16]	G20
55*	ETH2_MDI_B_P / GPIO2_IO[18] -No ETH PHY2	DS / IO	Gigabit Ethernet2 Positive Lane B/ General Purpose Input Output Register 2 Bit 18	GPIO2_IO[18]	DP83867IR_2.4 H21
56^	CSI1_DATA[5]	IO	Parallel Camera Data bit 5	GPIO3_IO[17]	F21
57*	ETH2_MDI_B_M / GPIO2_IO[19] -No ETH PHY2	DS / IO	Gigabit Ethernet2 Negative Lane B/ General Purpose Input Output Register 2 Bit 19	GPIO2_IO[19]	DP83867IR_2.5 H20
58^	CSI1_PIXCLK	IO	Parallel Camera Pixel clock	GPIO3_IO[11]	A24
59	GND	POWER	Digital GND		
60^	CSI1_DATA[2]	IO	Parallel Camera Data bit 2	GPIO3_IO[20]	C24
61*	ETH2_MDI_C_P / GPIO2_IO[21] -No ETH PHY2	DS / IO	Gigabit Ethernet2 Positive Lane C/ General Purpose Input Output Register 2 Bit 21	GPIO2_IO[21]	DP83867IR_2.7 G24
62^	CSI1_DATA[4]	IO	Parallel Camera Data bit 4	GPIO3_IO[18]	E22
63*	ETH2_MDI_C_M / GPIO2_IO[20] -No ETH PHY2	DS / IO	Gigabit Ethernet2 Negative Lane C/ General Purpose Input Output Register 2 Bit 20	GPIO2_IO[20]	DP83867IR_2.8 G25
64^	CSI1_DATA[7]	IO	Parallel Camera Data bit 7	GPIO3_IO[15]	B24
65	GND	POWER	Digital GND		
66^	CSI1_HSYNC	IO	Parallel Camera horizontal sync	GPIO3_IO[10]	B23
67*	ETH2_MDI_D_P / GPIO2_IO[22] -No ETH PHY2	DS / IO	Gigabit Ethernet2 Positive Lane D/ General Purpose Input Output Register 2 Bit 22	GPIO2_IO[22]	DP83867IR_2.10 H23
68^	CSI1_DATA[8]	IO	Parallel Camera Data bit 8	GPIO3_IO[14]	C23
69*	ETH2_MDI_D_M / GPIO2_IO[23] -No ETH PHY2	DS / IO	Gigabit Ethernet2 Negative Lane D/ General Purpose Input Output Register 2 Bit 23	GPIO2_IO[23]	DP83867IR_2.11 H22

Pin #	Signal	Type	Description	GPIO	Ball
70^	CSI1_VSYNC	IO	Parallel Camera vertical sync	GPIO3_IO[9])	C22
71	GND	POWER	Digital GND		
72^	CSI1_DATA[3]	IO	Parallel Camera Data bit 3	GPIO3_IO[19]	D23
73	GPIO2_IO[28]	IO	General Purpose Input Output Register 2 Bit 28	GPIO2_IO[28]	K24
74	GPIO2_IO[30]	IO	General Purpose Input Output Register 2 Bit 30	GPIO2_IO[30]	H24
75	GPIO2_IO[29]	IO	General Purpose Input Output Register 2 Bit 29	GPIO2_IO[29]	K23
76	GPIO2_IO[31]	IO	General Purpose Input Output Register 2 Bit 31	GPIO2_IO[31]	K20
77*	ETH2_LED_ACT / GPIO2_IO[24] -No ETH PHY2	O / IO	Gigabit Ethernet2 Activity LED / General Purpose Input Output Register 2 Bit 24	GPIO2_IO[24]	DP83867IR_2.45 (via inv. FET) J25
78	GND	POWER	Digital GND		
79*	ETH2_LED_LINK_1000 / GPIO2_IO[27] -No ETH PHY2	IO O / IO	Gigabit Ethernet2 Link 1000 LED / General Purpose Input Output Register 2 Bit 27	GPIO2_IO[27]	DP83867IR_2.47 H25
80	MIPI_CSI_D0_P	DS	MIPI CSI interface lane 0 positive		B16
81*	ETH2_LED_LINK_10_100 / GPIO2_IO[25] -No ETH PHY2	IO POWER/ IO	Gigabit Ethernet2 Link 10/100 LED / General Purpose Input Output Register 2 Bit 25	GPIO2_IO[25]	DP83867IR_2.GND J24
82	MIPI_CSI_D0_N	DS	MIPI CSI interface lane 0 negative		A16
83*	GPIO2_IO[26] -No ETH PHY2	IO	General Purpose Input Output Register 2 Bit 26	GPIO2_IO[26]	K21
84	GND	POWER	Digital GND		
85	GND	POWER	Digital GND		
86	MIPI_CSI_CLK_P	DS	MIPI CSI interface clock positive		B15
87	MIPI_DSI_D0_P	DS	MIPI DSI interface lane 0 positive		B20
88	MIPI_CSI_CLK_N	DS	MIPI CSI interface clock negative		A15
89	MIPI_DSI_D0_N	DS	MIPI DSI interface lane 0 negative		A20
90	GND	POWER	Digital GND		
91	GND	POWER	Digital GND		
92	MIPI_CSI_D1_P	DS	MIPI CSI interface lane 1 positive		B14
93	MIPI_DSI_CLK_P	DS	MIPI DSI interface clock positive		B19
94	MIPI_CSI_D1_N	DS	MIPI CSI interface lane 1 negative		A14
95	MIPI_DSI_CLK_N	DS	MIPI DSI interface clock negative		A19
96	GND	POWER	Digital GND		
97	GND	POWER	Digital GND		
98	USB_OTG2_DP	DS	USB OTG2 data PLUS		B10
99	MIPI_DSI_D1_P	DS	MIPI DSI interface lane 1 positive		B18
100	USB_OTG2_DN	DS	USB OTG2 data minus		A10
101	MIPI_DSI_D1_N	DS	MIPI DSI interface lane 1 negative		A18
102	USB_HOST_VBUS	I	USB HOST VBUS		C10
103	GND	POWER	Digital GND		
104	USB_OTG1_ID	I	USB OTG1 Host/Device mode detection		B07
105*	ETH1_MDI_A_P / GPIO7_IO[0] -No ETH PHY1	DS / IO	Gigabit Ethernet1 Positive Lane A / General Purpose Input Output Register 7 Bit 0	GPIO7_IO[0]	DP83867IR_1.1 E14
106	USB_OTG1_DP	DS	USB OTG1 data PLUS		B08

Pin #	Signal	Type	Description	GPIO	Ball
107*	ETH1_MDI_A_M / GPIO7_IO[1] -No ETH PHY1	DS / IO	Gigabit Ethernet1 Negative Lane A / General Purpose Input Output Register 7 Bit 1	GPIO7_IO[1]	DP83867IR_1.2 F14
108	USB_OTG1_DN	IO	USB OTG1 data MINUS		A08
109	GND	POWER	Digital GND		
110	USB_OTG_VBUS	I	USB OTG1 VBUS		C08
111*	ETH1_MDI_B_P / GPIO7_IO[2] -No ETH PHY1	DS / IO	Gigabit Ethernet1 Positive Lane B / General Purpose Input Output Register 7 Bit 2	GPIO7_IO[2]	DP83867IR_1.4 D13
112	HSIC_DATA	IO	high-speed inter-chip USB data		A12
113*	ETH1_MDI_B_M / GPIO7_IO[3] -No ETH PHY1	DS / IO	Gigabit Ethernet1 Negative Lane B / General Purpose Input Output Register 7 Bit 3	GPIO7_IO[3]	DP83867IR_1.5 E13
114	HSIC_STROBE	IO	high-speed inter-chip USB strobe		B12
115	GND	POWER	Digital GND		
116	GND	POWER	Digital GND		
117*	ETH1_MDI_C_P / GPIO7_IO[5] -No ETH PHY1	DS / IO	Gigabit Ethernet1 Positive Lane C / General Purpose Input Output Register 7 Bit 5	GPIO7_IO[5]	DP83867IR_1.7 F15
118	SD1_CD_B	IO		GPIO5_IO[0]	C06
119*	ETH1_MDI_C_M / GPIO7_IO[4] -No ETH PHY1	DS / IO	Gigabit Ethernet1 Negative Lane C / General Purpose Input Output Register 7 Bit 4	GPIO7_IO[4]	DP83867IR_1.8 E15
120	GPIO1_IO[13]	IO	General Purpose Input Output Register 1 Bit 13	GPIO1_IO[13]	T3
121	GND	POWER	Digital GND		
122	SD1_CMD	IO	SD Card 1 Interface Command Signal	GPIO5_IO[4]	C05
123*	ETH1_MDI_D_P / GPIO7_IO[6] -No ETH PHY1	DS / IO	Gigabit Ethernet1 Positive Lane D / General Purpose Input Output Register 7 Bit 6	GPIO7_IO[6]	DP83867IR_1.10 F17
124	SD1_DATA2	IO	SD Card 1 Interface Data 2 Signal	GPIO5_IO[7]	A04
125*	ETH1_MDI_D_M / GPIO7_IO[7] -No ETH PHY1	DS / IO	Gigabit Ethernet1 Negative Lane D / General Purpose Input Output Register 7 Bit 7	GPIO7_IO[7]	DP83867IR_1.11 E17
126	SD1_DATA1	IO	SD Card 1 Interface Data 1 Signal	GPIO5_IO[6]	D06
127	GND	POWER	Digital GND		
128	SD1_CLK	IO	SD Card 1 Interface clock Signal	GPIO5_IO[3]	B05
129*	ETH1_LED_ACT / GPIO7_IO[8] -No ETH PHY1	O / IO	Gigabit Ethernet1 Activity LED / General Purpose Input Output Register 7 Bit 8	GPIO7_IO[8]	DP83867IR_1.45 (via inv. FET) E18
130	SD1_DATA3	IO	SD Card 1 Interface Data 3 Signal	GPIO5_IO[8]	D05
131*	ETH1_LED_LINK_1000 / GPIO7_IO[11] -No ETH PHY1	IO O / IO	Gigabit Ethernet1 Link 1000 / General Purpose Input Output Register 7 Bit 11	GPIO7_IO[11]	DP83867IR_1.47 F16
132	SD1_DATA0	IO	SD Card 1 Interface Data 0 Signal	GPIO5_IO[5]	A05
133*	ETH1_LED_LINK_10_100 / GPIO7_IO[9] -No ETH PHY1	IO POWER/ IO	Gigabit Ethernet1 Link 10/100 / General Purpose Input Output Register 7 Bit 9	GPIO7_IO[9]	DP83867IR_1.GND D18
134	VCC_3V3	POWER	SOM Peripherals 3.3V		
135*	GPIO7_IO[10] -No ETH PHY1	IO	General Purpose Input Output Register 7 Bit 10	GPIO7_IO[10]	E16
136	LICELL	POWER	3.0V RTC back-up battery supply input		

Pin #	Signal	Type	Description	GPIO	Ball
137	VCC_3V3_IN	POWER	Main power supply,3.3V		
138	VCC_3V3_IN	POWER	Main power supply,3.3V		
139	VCC_3V3_IN	POWER	Main power supply,3.3V		
140	VCC_3V3_IN	POWER	Main power supply,3.3V		
141	VCC_3V3_IN	POWER	Main power supply,3.3V		
142	VCC_3V3_IN	POWER	Main power supply,3.3V		
143	VCC_3V3_IN	POWER	Main power supply,3.3V		
144	VCC_3V3_IN	POWER	Main power supply,3.3V		
145	VCC_3V3_IN	POWER	Main power supply,3.3V		
146	VCC_3V3_IN	POWER	Main power supply,3.3V		
147	ECSPI2_MISO	IO	ECSPI 2 Master In Slave Out	GPIO4_IO[22]	H06
148	MX7_ONOFF	I	iMX7 SoC ONOFF Signal		AC08
149	ECSPI2_MOSI	IO	ECSPI 2 Master Out Slave In	GPIO4_IO[21]	G06
150	VSNVS	POWER	RTC Domain 3.0V power rail Output		PF3000.34
151	ECSPI2_CS0	IO	ECSPI 2 Chip Select 0	GPIO4_IO[23]	J06
152	BT_UART3_RTS_B	IO	Bluetooth UART RTS signal – Must be NC if Wi-Fi is assembled and BT is enabled	GPIO4_IO[6]	M05
153	ECSPI2_SCLK	IO	ECSPI 2 Clock	GPIO4_IO[20]	J05
154	BT_UART3_CTS_B	IO	Bluetooth UART CTS signal – Must be NC if Wi-Fi is assembled and BT is enabled	GPIO4_IO[7]	M06
155	CAN2_TX	IO	CAN Bus interface 2 Transmit signal	GPIO4_IO[13]	K06
156	BT_UART3_RXD	IO	Bluetooth UART RX signal – Must be NC if Wi-Fi is assembled and BT is enabled	GPIO4_IO[4]	M01
157	CAN2_RX	IO	CAN Bus interface 2 Receive signal	GPIO4_IO[12]	K05
158	BT_UART3_TXD	IO	Bluetooth UART TX signal – Must be NC if Wi-Fi is assembled and BT is enabled	GPIO4_IO[5]	M02
159	UART1_RXD	IO	Debug UART RX signal	GPIO4_IO[0]	L03
160	POR_B	I O	iMX7 SoC Power On Reset Input signal, PMIC Reset open drain output signal		R06, PF3000.3
161	UART1_TXD	IO	Debug UART TX signal	GPIO4_IO[1]	L04
162	PMIC_PWRON	I	PMIC Power On signal – A delay should be added on PMIC_PWRON signal, see reference schematics.		PF3000.48
163	CLKO2	IO	Reference clock 2 out	GPIO5_IO[1]	C04
164	PMIC_STBY_REQ	O	iMX7 SoC Standby request output		AC07
165~	I2C1_SCL	IO	I2C Bus 1 Clock I2C1 bus is used for boot process - pins' mode Cannot be altered	GPIO4_IO[8]	J02
166	PMIC_ON_REQ	O	iMX7 SoC PMIC power on output		AB08
167~	I2C1_SDA	IO	I2C Bus 1 Data I2C1 bus is used for boot process - pins' mode Cannot be altered	GPIO4_IO[9]	K01
168	PWM2	IO	Pulse width modulation 2 signal	GPIO1_IO[2]	N03
169~	I2C2_SCL	IO	I2C Bus 2 Clock I2C2 bus is used by Audio codec – pins' mode Cannot be altered if Audio codec is assembled	GPIO4_IO[10	K02
170	GWDOG_RST_B	IO	Watch Dog Reset Input	GPIO1_IO[0]	N01
171~	I2C2_SDA	IO	I2C Bus 2 Data I2C2 bus is used by Audio codec – pins' mode Cannot be altered if Audio codec is assembled	GPIO4_IO [11]	K03

Pin #	Signal	Type	Description	GPIO	Ball
172	SAI2_RX_BCLK	IO	SAI2 Receive Bit Clock	GPIO6_IO[17]	D12
173	I2C4_SDA	IO	I2C Bus 4 Data	GPIO4_IO[15]	L02
174	SAI2_RX_DATA	IO	SAI2 Receive Data	GPIO6_IO[21]	E09
175	I2C4_SCL	IO	I2C Bus 4 Clock	GPIO4_IO[14]	L01
176	SAI2_RX_SYNC	IO	SAI2 Receive Frame Sync	GPIO6_IO[16]	C12
177	SAI2_TX_BCLK	IO	SAI2 Transmit Bit Clock	GPIO6_IO[20]	D08
178	SAI2_TX_DATA	IO	SAI2 Transmit Data	GPIO6_IO[22]	E8
179	SAI2_TX_SYNC	IO	SAI2 Transmit Frame Sync	GPIO6_IO[19]	D09
180	GND	POWER	Digital GND		
181	GPIO1_IO[10]	IO	General Purpose Input Output Register 1 Bit 10	GPIO1_IO[10]	R05
182	PCIE_TX_P	DS	PCI express Transmit Positive signal		AB11
183	GPIO1_IO[12]	IO	General Purpose Input Output Register 1 Bit 12	GPIO1_IO[12]	T2
184	PCIE_TX_N	DS	PCI express Transmit Negative signal		AC11
185	GPIO1_IO[11]	IO	General Purpose Input Output Register 1 Bit 11	GPIO1_IO[11]	T01
186	GND	POWER	Digital GND		
187~	OSC_32K_OUT	IO	Wi-Fi/BT Module 32K Reference clock – Function Must not be Altered if Wi-Fi/BT Module is assembled	GPIO1_IO[3]	N05
188	PCIE_REFCLK_P	DS	PCI express Reference clock input Positive signal		AD10
189	USB_OTG2_PWR	IO	USB OTG2 Power Enable	GPIO1_IO[7]	P03
190	PCIE_REFCLK_N	DS	PCI express Reference clock input Negative signal		AE10
191	USB_OTG1_PWR	IO	USB OTG1 Power Enable	GPIO1_IO[5]	P01
192	GND	POWER	Digital GND		
193	GND	POWER	Digital GND		
194	PCIE_REFCLKOUT_P	DS	PCI express Reference clock output Positive signal		AB10
195	ADC2_IN1	AI	Analog to Digital converter 2 Input 1 (1.8V)		AC02
196	PCIE_REFCLKOUT_N	DS	PCI express Reference clock output Negative signal		AC10
197	ADC2_IN2	AI	Analog to Digital converter 2 Input 2 (1.8V)		AB01
198	GND	POWER	Digital GND		
199	ADC2_IN0	AI	Analog to Digital converter 2 Input 0 (1.8V)		AC01
200	PCIE_RX_P	DS	PCI express Receive Positive signal		AD11
201	ADC2_IN3	AI	Analog to Digital converter 2 Input 3 (1.8V)		AB02
202	PCIE_RX_N	DS	PCI express Receive Negative signal		AE11
203	GND	POWER	Digital GND		
204	GND	POWER	Digital GND		

Notes:

[*] Pins marked with * are connected to iMX7 SoC balls only on specific subsets of SOMs. Otherwise, ball is connected to On SOM devices and pin is used to export devices' interface.

[^] Pins marked with ^ are being latched at boot to determine boot sequence. External drivers to this pin should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see Boot section.

[~] Pins marked with ~ are used by certain subsets of SOMs for internal SOM connections, Pin function must not be altered if using these subsets.

4.2. Pin Mux

The table below summarizes the additional available functionality for each pin in the SO-DIMM 204 pin connector.

PIN	i.MX7 Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8
1*	N02	gpio1.IO[1]	pwm1.OUT	ccm.ENET3_REF_CLK_ROOT	sai1.MCLK	anatop.24M_OUT				
2	L24	epdc.SDDO[10]	sim1.PORT1_RST_B	qspi.B_DATA[2]	uart6.RTS_B	weim.CS0_B	gpio2.IO[10]	lcdif.DATA[10]	lcdif.DATA[9]	epdc.SDOE
4	P21	epdc.SDDO[1]	sim1.PORT2_CLK	qspi.A_DATA[1]	kpp.COL[3]	weim.AD[1]	gpio2.IO[1]	lcdif.DATA[1]	lcdif.ENABLE	
6	N22	epdc.SDDO[4]	sim1.PORT2_PD	qspi.A_DQS	kpp.ROW[1]	weim.AD[4]	gpio2.IO[4]	lcdif.DATA[4]	sjc.FAIL	
7*	E19	enet1.CRS	wdog2.WDOG_RST_B_DEB	sai1.TX_SYNC	gpt2.CAPTURE1	epdc.PWRCTRL[0]	gpio7.IO[14]	ccm.EXT_CLK3	csu.CSU_ALARM_AUT[2]	
8	L25	epdc.SDDO[9]	sim1.PORT1_CLK	qspi.B_DATA[1]	uart6.TX	weim.RW	gpio2.IO[9]	lcdif.DATA[9]	lcdif.DATA[0]	epdc.SDLE
9*	D16	enet1.TX_CLK	ccm.ENET1_REF_CLK_ROOT	sai1.RX_DATA[0]	gpt2.COMPARE3	epdc.PWRIRQ	gpio7.IO[12]	ccm.EXT_CLK1	csu.CSU_ALARM_AUT[0]	
10	K25	epdc.SDDO[15]	sim2.PORT1_RST_B	qspi.B_SS1_B	uart7.CTS_B	weim.CS1_B	gpio2.IO[15]	lcdif.DATA[15]	lcdif.WR_RWN	epdc.PWRCOM
12	N21	epdc.SDDO[3]	sim1.PORT2_SVEN	qspi.A_DATA[3]	kpp.COL[2]	weim.AD[3]	gpio2.IO[3]	lcdif.DATA[3]	lcdif.HSYNC	
13*	D15	enet1.RX_CLK	wdog2.WDOG_B	sai1.TX_BCLK	gpt2.CLK	epdc.PWRWAKE	gpio7.IO[13]	ccm.EXT_CLK2	csu.CSU_ALARM_AUT[1]	
14	N20	epdc.SDDO[2]	sim1.PORT2_RST_B	qspi.A_DATA[2]	kpp.ROW[2]	weim.AD[2]	gpio2.IO[2]	lcdif.DATA[2]	lcdif.VSYNC	
15*	D19	enet1.COL	global wdog	sai1.TX_DATA[0]	gpt2.CAPTURE2	epdc.PWRCTRL[1]	gpio7.IO[15]	ccm.EXT_CLK4	csu.CSU_INT_DEB	
16	P20	epdc.SDDO[0]	sim1.PORT2_TRXD	qspi.A_DATA[0]	kpp.ROW[3]	weim.AD[0]	gpio2.IO[0]	lcdif.DATA[0]	lcdif.CLK	
17	M23	epdc.SDDO[8]	sim1.PORT1_TRXD	qspi.B_DATA[0]	uart6.RX	weim.OE	gpio2.IO[8]	lcdif.DATA[8]	lcdif.BUSY	epdc.SDCLK
18	L23	epdc.SDDO[11]	sim1.PORT1_SVEN	qspi.B_DATA[3]	uart6.CTS_B	weim.BCLK	gpio2.IO[11]	lcdif.DATA[11]	lcdif.DATA[1]	epdc.SDCE0
19	M22	epdc.SDDO[7]	sim2.PORT2_RST_B	qspi.A_SS1_B	kpp.COL[0]	weim.AD[7]	gpio2.IO[7]	lcdif.DATA[7]	sjc.DONE	
20	D25	lcdif.DATA[22]	flextimer2.CH[6]	enet2.1588_EVENT2_OUT	csi1.DATA[11]	weim.ADDR[25]	gpio3.IO[27]	I2C4_SCL		
21	M21	epdc.SDDO[6]	sim2.PORT2_CLK	qspi.A_SS0_B	kpp.ROW[0]	weim.AD[6]	gpio2.IO[6]	lcdif.DATA[6]	sjc.DE_B	
22	E24	lcdif.DATA[21]	flextimer2.CH[5]	enet1.1588_EVENT3_OUT	csi1.DATA[12]	weim.ADDR[24]	gpio3.IO[26]	I2C3_SDA	sim_m.HADDR[21]	
23^	A22	lcdif.DATA[1]	gpt1.COMPARE3		csi1.DATA[21]	weim.DATA[1]	gpio3.IO[6]	src.BT_CFG[1]		
24	L20	epdc.SDDO[14]	sim2.PORT1_CLK	qspi.B_SS0_B	uart7.RTS_B	weim.EB_B[0]	gpio2.IO[14]	lcdif.DATA[14]	lcdif.DATA[22]	epdc.GDSP
25	L22	epdc.SDDO[12]	sim1.PORT1_PD	qspi.B_DQS	uart7.RX	weim.LBA_B	gpio2.IO[12]	lcdif.DATA[12]	lcdif.DATA[21]	epdc.GDCLK

PIN	i.MX7 Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8
26	G23	lcdif.DATA[23]	flextimer2.CH[7]	enet2.1588_EVENT3_OUT	csi1.DATA[10]	weim.ADDR[26]	gpio3.IO[28]	I2C4_SDA		
27^	B22	lcdif.DATA[2]	gpt1.CLK		csi1.DATA[22]	weim.DATA[2]	gpio3.IO[7]	src.BT_CFG[2]		
28^	D24	lcdif.DATA[19]	flextimer1.CH[7]		csi1.DATA[14]	weim.CS3_B	gpio3.IO[24]	src.BT_CFG[19]		
29^	B25	lcdif.DATA[16]	flextimer1.CH[4]		csi1.DATA[1]	weim.CRE	gpio3.IO[21]	src.BT_CFG[16]		
30	C25	lcdif.DATA[20]	flextimer2.CH[4]	enet1.1588_EVENT2_OUT	csi1.DATA[13]	weim.ADDR[23]	gpio3.IO[25]	I2C3_SCL		
31^	A23	lcdif.DATA[3]	gpt1.CAPTURE1		csi1.DATA[23]	weim.DATA[3]	gpio3.IO[8]	src.BT_CFG[3]		
32	M20	epdc.SDDO[5]	sim2.PORT2_TRXD	qspi.A_SCLK	kpp.COL[1]	weim.AD[5]	gpio2.IO[5]	lcdif.DATA[5]	sjc.JTAG_ACT	
33^	E23	lcdif.DATA[18]	flextimer1.CH[6]	coresight.EVENTO	csi1.DATA[15]	weim.CS2_B	gpio3.IO[23]	src.BT_CFG[18]		
34	L21	epdc.SDDO[13]	sim2.PORT1_TRXD	qspi.B_SCLK	uart7.TX	weim.WAIT	gpio2.IO[13]	lcdif.DATA[13]	lcdif.CS	epdc.GDOE
36	C21	lcdif.RESET	gpt1.COMPARE1	coresight.EVENTI	csi1.FIELD	weim.DTACK_B	gpio3.IO[4]			
38^	G21	lcdif.DATA[17]	flextimer1.CH[5]		csi1.DATA[0]	weim.ACLK_FREERUN	gpio3.IO[22]	src.BT_CFG[17]		
40^	D21	lcdif.DATA[0]	gpt1.COMPARE2		csi1.DATA[20]	weim.DATA[0]	gpio3.IO[5]	src.BT_CFG[0]		
42	F25	lcdif.ENABLE	ecspi4.MOSI	enet1.1588_EVENT3_IN	csi1.DATA[17]	uart2.TX	gpio3.IO[1]		sim_m.HPROT[0]	
43~	D03	usdhc2.CD_B	enet1.MDIO	enet2.MDIO	ecspi3.SS2	flextimer1.PHB	gpio5.IO[9]	sdma.EXT_EVENT[0]		
44	E25	lcdif.HSYNC	ecspi4.SCLK	enet2.1588_EVENT2_IN	csi1.DATA[18]	uart2.RTS_B	gpio3.IO[2]			
45~	C03	usdhc2.WP	enet1.MDC	enet2.MDC	ecspi3.SS3	usb.OTG1_ID	gpio5.IO[10]	sdma.EXT_EVENT[1]		
46	F24	lcdif.VSYNC	ecspi4.SS0	enet2.1588_EVENT3_IN	csi1.DATA[19]	uart2.CTS_B	gpio3.IO[3]			
48	E20	lcdif.CLK	ecspi4.MISO	enet1.1588_EVENT2_IN	csi1.DATA[16]	uart2.RX	gpio3.IO[0]			
49*	J21	epdc.SDCLK	sim2.PORT2_SVEN	enet2.RGMII_RD0	kpp.ROW[4]	weim.AD[10]	gpio2.IO[16]	lcdif.CLK	lcdif.DATA[20]	
50^	F20	lcdif.DATA[7]			csi1.MCLK	weim.DATA[7]	gpio3.IO[12]	src.BT_CFG[7]		
51*	J20	epdc.SDLE	sim2.PORT2_PD	enet2.RGMII_RD1	kpp.COL[4]	weim.AD[11]	gpio2.IO[17]	lcdif.DATA[16]	lcdif.DATA[8]	
52^	E21	lcdif.DATA[8]			csi1.DATA[9]	weim.DATA[8]	gpio3.IO[13]	src.BT_CFG[8]		
54^	G20	lcdif.DATA[11]			csi1.DATA[6]	weim.DATA[11]	gpio3.IO[16]	src.BT_CFG[11]		
55*	H21	epdc.SDOE	flextimer1.CH[0]	enet2.RGMII_RD2	kpp.COL[5]	weim.AD[12]	gpio2.IO[18]	lcdif.DATA[17]	lcdif.DATA[23]	
56^	F21	lcdif.DATA[12]			csi1.DATA[5]	weim.DATA[12]	gpio3.IO[17]	src.BT_CFG[12]		
57*	H20	epdc.SDSHR	flextimer1.CH[1]	enet2.RGMII_RD3	kpp.ROW[5]	weim.AD[13]	gpio2.IO[19]	lcdif.DATA[18]	lcdif.DATA[10]	

PIN	i.MX7 Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8
58^	A24	lcdif.DATA[6]			csi1.PIXCLK	weim.DATA[6]	gpio3.IO[11]	src.BT_CFG[6]		
60^	C24	lcdif.DATA[15]			csi1.DATA[2]	weim.DATA[15]	gpio3.IO[20]	src.BT_CFG[15]		
61*	G24	epdc.SDCE[1]	flextimer1.CH[3]	enet2.RGMII_RXC	enet2.RX_ER	weim.AD[15]	gpio2.IO[21]	lcdif.DATA[20]	lcdif.DATA[4]	
62^	E22	lcdif.DATA[13]			csi1.DATA[4]	weim.DATA[13]	gpio3.IO[18]	src.BT_CFG[13]		
63*	G25	epdc.SDCE[0]	flextimer1.CH[2]	enet2.RGMII_RX_CTL		weim.AD[14]	gpio2.IO[20]	lcdif.DATA[19]	lcdif.DATA[5]	
64^	B24	lcdif.DATA[10]			csi1.DATA[7]	weim.DATA[10]	gpio3.IO[15]	src.BT_CFG[10]		
66^	B23	lcdif.DATA[5]			csi1.HSYNC	weim.DATA[5]	gpio3.IO[10]	src.BT_CFG[5]		
67*	H23	epdc.SDCE[2]	sim2.PORT1_SVEN	enet2.RGMII_TD0	kpp.COL[6]	weim.ADDR[16]	gpio2.IO[22]	lcdif.DATA[21]	lcdif.DATA[3]	
68^	C23	lcdif.DATA[9]			csi1.DATA[8]	weim.DATA[9]	gpio3.IO[14]	src.BT_CFG[9]		
69*	H22	epdc.SDCE[3]	sim2.PORT1_PD	enet2.RGMII_TD1	kpp.ROW[6]	weim.ADDR[17]	gpio2.IO[23]	lcdif.DATA[22]	lcdif.DATA[2]	
70^	C22	lcdif.DATA[4]	gpt1.CAPTURE2		csi1.VSYNC	weim.DATA[4]	gpio3.IO[9]	src.BT_CFG[4]		
72^	D23	lcdif.DATA[14]			csi1.DATA[3]	weim.DATA[14]	gpio3.IO[19]	src.BT_CFG[14]		
73	K24	epdc.BDR[0]		enet2.TX_CLK	ccm.ENET2_REF_CLK_ROOT	weim.ADDR[22]	gpio2.IO[28]	lcdif.CS	lcdif.DATA[7]	
74	H24	epdc.PWRCOM	flextimer2.PHA	enet2.CRS		weim.AD[9]	gpio2.IO[30]	lcdif.HSYNC	lcdif.DATA[11]	
75	K23	epdc.BDR[1]	epdc.SDCLKN	enet2.RX_CLK		weim.AD[8]	gpio2.IO[29]	lcdif.ENABLE	lcdif.DATA[6]	
76	K20	epdc.PWRSTAT	flextimer2.PHB	enet2.COL		weim.EB_B[1]	gpio2.IO[31]	lcdif.VSYNC	lcdif.DATA[12]	
77*	J25	epdc.GDCLK	flextimer2.CH[0]	enet2.RGMII_TD2	kpp.COL[7]	weim.ADDR[18]	gpio2.IO[24]	lcdif.DATA[23]	lcdif.DATA[16]	
79*	H25	epdc.GDSP	flextimer2.CH[3]	enet2.RGMII_TXC	enet2.TX_ER	weim.ADDR[21]	gpio2.IO[27]	lcdif.BUSY	lcdif.DATA[17]	
81*	J24	epdc.GDOE	flextimer2.CH[1]	enet2.RGMII_TD3	kpp.ROW[7]	weim.ADDR[19]	gpio2.IO[25]	lcdif.WR_RWN	lcdif.DATA[18]	
83*	K21	epdc.GDRL	flextimer2.CH[2]	enet2.RGMII_TX_CTL		weim.ADDR[20]	gpio2.IO[26]	lcdif.RD_E	lcdif.DATA[19]	
105*	E14	enet1.RGMII_RD0	pwm1.OUT	i2c3.SCL	uart1.CTS_B	epdc.VCOM[0]	gpio7.IO[0]	kpp.ROW[3]		
107*	F14	enet1.RGMII_RD1	pwm2.OUT	i2c3.SDA	uart1.RTS_B	epdc.VCOM[1]	gpio7.IO[1]	kpp.COL[3]		
111*	D13	enet1.RGMII_RD2	can1.RX	ecspi2.SCLK	uart1.RX	epdc.SDCE[4]	gpio7.IO[2]	kpp.ROW[2]		
113*	E13	enet1.RGMII_RD3	can1.TX	ecspi2.MOSI	uart1.TX	epdc.SDCE[5]	gpio7.IO[3]	kpp.COL[2]		
117*	F15	enet1.RGMII_RXC	enet1.RX_ER	ecspi2.SS2		epdc.SDCE[7]	gpio7.IO[5]	kpp.COL[1]		
118	C06	usdhc1.CD_B		uart6.RX	ecspi4.MISO	flextimer1.CH[0]	gpio5.IO[0]	ccm.CLKO1		

PIN	i.MX7 Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8
119*	E15	enet1.RGMII_RX_CTL		ecspi2.SS1		epdc.SDCE[6]	gpio7.IO[4]	kpp.ROW[1]		
120	T3	gpio1.IO[13]	usdhc3.VSELECT	ccm.ENET2_REF_CLK_ROOT	can1.TX	gpc.PMIC_RDY	ccm.EXT_CLK2	snvs_hp_wrapper.VIO_5_CTL	usb.OTG2_ID	
122	C05	usdhc1.CMD	sai3.RX_BCLK		ecspi4.SS1	flextimer2.CH[0]	gpio5.IO[4]			
123*	F17	enet1.RGMII_TD0	pwm3.OUT	ecspi2.SS3		epdc.SDCE[8]	gpio7.IO[6]	kpp.ROW[0]		
124	A04	usdhc1.DATA2	sai3.TX_SYNC	uart7.CTS_B	ecspi4.RDY	flextimer2.CH[3]	gpio5.IO[7]	ccm.EXT_CLK3		
125*	E17	enet1.RGMII_TD1	pwm4.OUT	ecspi2.RDY		epdc.SDCE[9]	gpio7.IO[7]	kpp.COL[0]		
126	D06	usdhc1.DATA1	sai3.TX_BCLK	uart7.TX	ecspi4.SS3	flextimer2.CH[2]	gpio5.IO[6]	ccm.EXT_CLK2		
128	B05	usdhc1.CLK	sai3.RX_SYNC	uart6.CTS_B	ecspi4.SS0	flextimer1.CH[3]	gpio5.IO[3]			
129*	E18	enet1.RGMII_TD2	can2.RX	ecspi2.MISO	i2c4.SCL	epdc.SDOED	gpio7.IO[8]			
130	D05	usdhc1.DATA3	sai3.TX_DATA[0]	uart7.RTS_B	ecspi3.SS1	flextimer1.PHA	gpio5.IO[8]	ccm.EXT_CLK4		
131*	F16	enet1.RGMII_TXC	enet1.TX_ER	sai1.RX_BCLK	gpt2.COMPARE2	epdc.PWRCTRL[3]	gpio7.IO[11]			
132	A05	usdhc1.DATA0	sai3.RX_DATA[0]	uart7.RX	ecspi4.SS2	flextimer2.CH[1]	gpio5.IO[5]	ccm.EXT_CLK1		
133*	D18	enet1.RGMII_TD3	can2.TX	ecspi2.SS0	i2c4.SDA	epdc.SDOEZ	gpio7.IO[9]		caam_wrapper.RNG_OSC_OBS	
135*	E16	enet1.RGMII_TX_CTL		sai1.RX_SYNC	gpt2.COMPARE1	epdc.PWRCTRL[2]	gpio7.IO[10]			
147	H06	ecspi2.MISO	uart7.RTS_B	usdhc1.DATA6	csi1.DATA[8]	lcdif.DATA[15]	gpio4.IO[22]	epdc.PWRCTRL[2]		
149	G06	ecspi2.MOSI	uart7.TX	usdhc1.DATA5	csi1.DATA[7]	lcdif.DATA[14]	gpio4.IO[21]	epdc.PWRCTRL[1]		
151	J06	ecspi2.SS0	uart7.CTS_B	usdhc1.DATA7	csi1.DATA[9]	lcdif.RESET	gpio4.IO[23]	epdc.PWRWAKE		
152	M05	uart3.RTS_B	usb.OTG2_OC	sai3.TX_DATA[0]	ecspi1.SCLK	enet1.1588_EVENT1_IN	gpio4.IO[6]	usdhc3.LCTL		
153	J05	ecspi2.SCLK	uart7.RX	usdhc1.DATA4	csi1.DATA[6]	lcdif.DATA[13]	gpio4.IO[20]	epdc.PWRCTRL[0]		
154	M06	uart3.CTS_B	usb.OTG2_PWR	sai3.TX_SYNC	ecspi1.SS0	enet1.1588_EVENT1_OUT	gpio4.IO[7]	usdhc1.VSELECT		
155	K06	i2c3.SDA	uart5.RTS_B	can2.TX	csi1.HSYNC	sdma.EXT_EVENT[1]	gpio4.IO[13]	epdc.BDR[1]		
156	M01	uart3.RX	usb.OTG1_OC	sai3.RX_SYNC	ecspi1.MISO	enet1.1588_EVENT0_IN	gpio4.IO[4]	usdhc1.LCTL		
157	K05	i2c3.SCL	uart5.CTS_B	can2.RX	csi1.VSYNC	sdma.EXT_EVENT[0]	gpio4.IO[12]	epdc.BDR[0]		
158	M02	uart3.TX	usb.OTG1_PWR	sai3.TX_BCLK	ecspi1.MOSI	enet1.1588_EVENT0_OUT	gpio4.IO[5]	usdhc2.LCTL		

PIN	i.MX7 Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8
159	L03	uart1.RX	i2c1.SCL	gpc.PMIC_RDY	ecspi1.SS1	enet2.1588_EVENT0_IN	gpio4.IO[0]	enet1.MDIO		
161	L04	uart1.TX	i2c1.SDA	sai3.MCLK	ecspi1.SS2	enet2.1588_EVENT0_OUT	gpio4.IO[1]	enet1.MDC		
163	C04	usdhc1.WP		uart6.TX	ecspi4.MOSI	flextimer1.CH[1]	gpio5.IO[1]	ccm.CLKO2		
165~	J02	i2c1.SCL	uart4.CTS_B	can1.RX	ecspi3.MISO		gpio4.IO[8]	usdhc2.VSELECT		
167~	K01	i2c1.SDA	uart4.RTS_B	can1.TX	ecspi3.MOSI	ccm.ENET1_REF_CLK_ROOT	gpio4.IO[9]	usdhc3.VSELECT		
168	N03	gpio1.IO[2]	pwm2.OUT	ccm.ENET1_REF_CLK_ROOT	sai2.MCLK	anatop.32K_OUT	ccm.CLKO1		usb.OTG1_ID	
169~	K02	i2c2.SCL	uart4.RX	wdog3.WDOG_B	ecspi3.SCLK	ccm.ENET2_REF_CLK_ROOT	gpio4.IO[10]	usdhc3.CD_B		
170	N01	gpio1.IO[0]	pwm4.OUT	global wdog	wdog1.WDOG_B	wdog1.WDOG_RST_B_DEB				
171~	K03	i2c2.SDA	uart4.TX	wdog3.WDOG_RST_B_DEB	ecspi3.SS0	ccm.ENET3_REF_CLK_ROOT	gpio4.IO[11]	usdhc3.WP		
172	D12	sai1.RX_BCLK	rawnand.CE3_B	sai2.RX_BCLK	i2c4.SDA	flextimer2.PHA	gpio6.IO[17]			
173~	L02	i2c4.SDA	uart5.TX	wdog4.WDOG_RST_B_DEB	csi1.MCLK	usb.OTG2_ID	gpio4.IO[15]	epdc.VCOM[1]		
174	E09	sai2.RX_DATA[0]	ecspi3.SCLK	uart4.CTS_B	uart2.CTS_B	flextimer2.CH[6]	gpio6.IO[21]	kpp.COL[7]		
175	L01	i2c4.SCL	uart5.RX	wdog4.WDOG_B	csi1.PIXCLK	usb.OTG1_ID	gpio4.IO[14]	epdc.VCOM[0]		
176	C12	sai1.RX_SYNC	rawnand.CE2_B	sai2.RX_SYNC	i2c4.SCL	sim1.PORT1_PD	gpio6.IO[16]	mqs.RIGHT	src.CA7_CORERESET_N[0]	
177	D08	sai2.TX_BCLK	ecspi3.MOSI	uart4.TX	uart1.RTS_B	flextimer2.CH[5]	gpio6.IO[20]			
178	E8	sai2.TX_DATA[0]	ecspi3.SS0	uart4.RTS_B	uart2.RTS_B	flextimer2.CH[7]	gpio6.IO[22]	kpp.ROW[7]		
179	D09	sai2.TX_SYNC	ecspi3.MISO	uart4.RX	uart1.CTS_B	flextimer2.CH[4]	gpio6.IO[19]			
181	R05	gpio1.IO[10]	usdhc2.LCTL	enet1.MDIO	uart3.RTS_B	i2c4.SCL	flextimer1.PHA	kpp.COL[6]	pwm3.OUT	
183	T2	gpio1.IO[12]	usdhc2.VSELECT	ccm.ENET1_REF_CLK_ROOT	can1.RX	m4.NMI	ccm.EXT_CLK1	snvs_hp_wrapper.VIO_5	usb.OTG1_ID	
185	T01	gpio1.IO[11]	usdhc3.LCTL	enet1.MDC	uart3.CTS_B	i2c4.SDA	flextimer1.PHB	kpp.ROW[6]	pwm4.OUT	
187~	N05	gpio1.IO[3]	pwm3.OUT	ccm.ENET2_REF_CLK_ROOT	sai3.MCLK	osc32k.32K_OUT	ccm.CLKO2		usb.OTG2_ID	
189	P03	gpio1.IO[7]	usb.OTG2_PWR	flextimer1.CH[7]	uart5.TX	i2c2.SDA	gpc.STOP	kpp.COL[4]		

PIN	i.MX7 Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8
191	P01	gpio1.IO[5]	usb.OTG1_PWR	flextimer1.CH[5]	uart5.RTS_B	i2c1.SDA				

Notes:

[*]Pins marked with * are connected to iMX7 SoC balls only on specific subsets of SOMs. Otherwise, ball is connected to On SOM devices and pin is used to export devices' interface.

[^] Pins marked with ^ are being latched at boot to determine boot sequence. External drivers to this pin should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see Boot section.

[~] Pins marked with ~ are used by certain subsets of SOMs for internal SOM connections, Pin function must not be altered if using these subsets.

5. SOM's interfaces

5.1. Display Interfaces

The VAR-SOM-MX7-5G_V2 consists of the following display interfaces:

- EPDC – Supporting direct-driver for E-Ink EPD panels with up to 2048 x 1536 at 106 Hz refresh (or 4096 x 4096 at 20 Hz)
- One parallel 24-bit display port with resolution up to 1920x1080at 60 Hz
- One MIPI DSI port supporting two data lanes and 1 clock lane with maximum bit rate of 1.5 Gbps

5.1.1. EPDC

The SOM exposes one EPDC (Electrophoretic Display Controller) interface.
The EPDC is a feature-rich, low power and high performance direct drive active matrix EPD controller. It is specifically designed to drive E•INK EPD panels supporting a wide variety of TFT backplanes.

The key features of the EPDC capabilities are:

- TFT resolutions up to 4096 x 4096 pixels with 20 Hz refresh (programmable up to 8191 x 8191)
- TFT resolutions up to 1650 x 2332 pixels at 106 Hz refresh
- Industry standard bus interfaces (AMBA AXI and APB)
- Up to 5-bit pixel representation for up to 32 greyscale levels
- Up to 64 concurrent updates with partial update support, except for 32(5-bit) grey level panel for which only 16 concurrent updates can be used
- Automatic collision handling when used in conjunction with the i.MX device driver
- Dual-scan TFT drive mode to support ultra-high resolution/refresh rate displays

Note: EPDC Interface is available only on iMX7D based SOMs and requires special SOM configuration.
Please contact sales@variscite.com for more information

EPDC signals:

Function	Pin #	Type	Description
EPDC_DATA[0]	16	O	Source Driver-Shift signal
EPDC_BDR[0]	73	O	Panel-Border Control (SW controlled)
EPDC_BDR[0]	157	O	Panel-Border Control (SW controlled)
EPDC_BDR[1]	75	O	Panel-Border Control (SW controlled)
EPDC_BDR[1]	155	O	Panel-Border Control (SW controlled)
EPDC_DATA[1]	4	O	Source Driver-Shift signal
EPDC_DATA[10]	2	O	Source Driver-Shift signal
EPDC_DATA[11]	18	O	Source Driver-Shift signal
EPDC_DATA[12]	25	O	Source Driver-Shift signal
EPDC_DATA[13]	34	O	Source Driver-Shift signal
EPDC_DATA[14]	24	O	Source Driver-Shift signal
EPDC_DATA[15]	10	O	Source Driver-Shift signal
EPDC_DATA[2]	14	O	Source Driver-Shift signal
EPDC_DATA[3]	12	O	Source Driver-Shift signal
EPDC_DATA[4]	6	O	Source Driver-Shift signal
EPDC_DATA[5]	32	O	Source Driver-Shift signal
EPDC_DATA[6]	21	O	Source Driver-Shift signal
EPDC_DATA[7]	19	O	Source Driver-Shift signal
EPDC_DATA[8]	17	O	Source Driver-Shift signal
EPDC_DATA[9]	8	O	Source Driver-Shift signal
EPDC_GDCLK	25	O	Gate Driver-Clock
EPDC_GDCLK	77*	O	Gate Driver-Clock
EPDC_GDOE	34	O	Gate Driver-Output Enable
EPDC_GDOE	81*	O	Gate Driver-Output Enable
EPDC_GDRL	83*	O	Gate Driver-Shift direction
EPDC_GDSP	24	O	Gate Driver-Start Pulse
EPDC_GDSP	79*	O	Gate Driver-Start Pulse
EPDC_PWRCOM	10	O	Panel-Power control (SW controlled)
EPDC_PWRCOM	74	O	Panel-Power control (SW controlled)
EPDC_PWRCTRL[0]	7*	O	Panel-Power control (SW controlled)
EPDC_PWRCTRL[1]	149	O	Panel-Power control (SW controlled)
EPDC_PWRCTRL[1]	15*	O	Panel-Power control (SW controlled)
EPDC_PWRCTRL[2]	147	O	Panel-Power control (SW controlled)
EPDC_PWRCTRL[2]	135*	O	Panel-Power control (SW controlled)
EPDC_PWRCTRL[3]	153	O	Panel-Power control (SW controlled)
EPDC_PWRCTRL[3]	131*	O	Panel-Power control (SW controlled)
EPDC_PWRIRQ	9*	O	Panel-Power irq
EPDC_PWRSTAT	76	O	Panel-Power status good
EPDC_PWRWAKE	151	O	Panel-Power control wake signal (SW controlled)
EPDC_PWRWAKE	13*	O	Panel-Power control wake signal (SW controlled)
EPDC_SDCE[0]	18	O	Source Driver-Chip-enable/StartPulse
EPDC_SDCE[0]	63*	O	Source Driver-Chip-enable/StartPulse
EPDC_SDCE[1]	61*	O	Source Driver-Chip-enable/StartPulse
EPDC_SDCE[2]	67*	O	Source Driver-Chip-enable/StartPulse
EPDC_SDCE[3]	69*	O	Source Driver-Chip-enable/StartPulse
EPDC_SDCE[4]	111*	O	Source Driver-Chip-enable/StartPulse
EPDC_SDCE[5]	113*	O	Source Driver-Chip-enable/StartPulse

Function	Pin #	Type	Description
EPDC_SDCE[6]	119*	O	Source Driver-Chip-enable/StartPulse
EPDC_SDCE[7]	117*	O	Source Driver-Chip-enable/StartPulse
EPDC_SDCE[8]	123*	O	Source Driver-Chip-enable/StartPulse
EPDC_SDCE[9]	125*	O	Source Driver-Chip-enable/StartPulse
EPDC_SDCLK	17	O	Positive Source Driver-Shift Clock
EPDC_SDCLK	49*	O	Positive Source Driver-Shift Clock
EPDC_SDLE	8	O	Source Driver-Latch Enable
EPDC_SDLE	51*	O	Source Driver-Latch Enable
EPDC_SDOE	2	O	Source Driver-Output Enable
EPDC_SDOE	55*	O	Source Driver-Output Enable
EPDC_SDOED	129*	O	Source Driver-Output Enable (to VDD)
EPDC_SDOEZ	133*	O	Source Driver-Output Enable (to Zero)
EPDC_SDSHR	57*	O	Source Driver-Shift dir
EPDC_VCOM[0]	175	O	Panel-VCOM
EPDC_VCOM[0]	105*	O	Panel-VCOM
EPDC_VCOM[1]	173	O	Panel-VCOM
EPDC_VCOM[1]	107*	O	Panel-VCOM

Note:

[*]Pins marked with * are connected to iMX7 SoC balls only on specific subsets of SOMs. Otherwise, ball is connected to On SOM devices and pin is used to export devices' interface.

4.1.2 Parallel Display

The SOM exposes one 24bit LCD interface with the following capabilities:

- Bus master interface to source frame buffer data for display refresh and a DMA interface to manage input data transfers from the LCD requiring minimal CPU overhead.
- 8/16/18/24 bit LCD data bus support available depending on I/O mux options.
- Programmable timing and parameters for MPU, VSYNC and DOTCLK LCD interfaces to support a wide variety of displays.
- ITU-R BT.656 mode (called Digital Video Interface or DVI mode here) including Progressive-to-interlace feature and RGB to YCbCr 4:2:2 color space conversion to support 525/60 and 625/50 operation.

Parallel Display signals:

Function	Pin #	Type	Description
LCD_BUSY	79*	I	LCD Interface Busy Signal
LCD_BUSY	17	I	LCD Interface Busy Signal
LCD_CLK	49*	O	LCD Interface Pixel Clock
LCD_CLK	48	O	LCD Interface Pixel Clock
LCD_CLK	16	O	LCD Interface Pixel Clock
LCD_CS	73	O	LCD Interface Chip Select
LCD_CS	34	O	LCD Interface Chip Select
LCD_DATA[0]	16	O	LCD Interface Data 0
LCD_DATA[0]	40^	O	LCD Interface Data 0
LCD_DATA[0]	8	O	LCD Interface Data 0
LCD_DATA[1]	4	O	LCD Interface Data 1

Function	Pin #	Type	Description
LCD_DATA[1]	23^	O	LCD Interface Data 1
LCD_DATA[1]	18	O	LCD Interface Data 1
LCD_DATA[10]	64^	O	LCD Interface Data 10
LCD_DATA[10]	2	O	LCD Interface Data 10
LCD_DATA[10]	57*	O	LCD Interface Data 10
LCD_DATA[11]	54^	O	LCD Interface Data 11
LCD_DATA[11]	18	O	LCD Interface Data 11
LCD_DATA[11]	74	O	LCD Interface Data 11
LCD_DATA[12]	56^	O	LCD Interface Data 12
LCD_DATA[12]	25	O	LCD Interface Data 12
LCD_DATA[12]	76	O	LCD Interface Data 12
LCD_DATA[13]	62^	O	LCD Interface Data 13
LCD_DATA[13]	34	O	LCD Interface Data 13
LCD_DATA[13]	153	O	LCD Interface Data 13
LCD_DATA[14]	72^	O	LCD Interface Data 14
LCD_DATA[14]	24	O	LCD Interface Data 14
LCD_DATA[14]	149	O	LCD Interface Data 14
LCD_DATA[15]	60^	O	LCD Interface Data 15
LCD_DATA[15]	10	O	LCD Interface Data 15
LCD_DATA[15]	147	O	LCD Interface Data 15
LCD_DATA[16]	51*	O	LCD Interface Data 16
LCD_DATA[16]	29^	O	LCD Interface Data 16
LCD_DATA[16]	77*	O	LCD Interface Data 16
LCD_DATA[17]	55*	O	LCD Interface Data 17
LCD_DATA[17]	38^	O	LCD Interface Data 17
LCD_DATA[17]	79*	O	LCD Interface Data 17
LCD_DATA[18]	57*	O	LCD Interface Data 18
LCD_DATA[18]	33^	O	LCD Interface Data 18
LCD_DATA[18]	81*	O	LCD Interface Data 18
LCD_DATA[19]	63*	O	LCD Interface Data 19
LCD_DATA[19]	28^	O	LCD Interface Data 19
LCD_DATA[19]	83*	O	LCD Interface Data 19
LCD_DATA[2]	14	O	LCD Interface Data 2
LCD_DATA[2]	27^	O	LCD Interface Data 2
LCD_DATA[2]	69*	O	LCD Interface Data 2
LCD_DATA[20]	61*	O	LCD Interface Data 20
LCD_DATA[20]	30^	O	LCD Interface Data 20
LCD_DATA[20]	49*	O	LCD Interface Data 20
LCD_DATA[21]	67*	O	LCD Interface Data 21
LCD_DATA[21]	22^	O	LCD Interface Data 21
LCD_DATA[21]	25	O	LCD Interface Data 21
LCD_DATA[22]	69*	O	LCD Interface Data 22
LCD_DATA[22]	20^	O	LCD Interface Data 22
LCD_DATA[22]	24	O	LCD Interface Data 22
LCD_DATA[23]	77*	O	LCD Interface Data 23
LCD_DATA[23]	26^	O	LCD Interface Data 23
LCD_DATA[23]	55*	O	LCD Interface Data 23
LCD_DATA[3]	12	O	LCD Interface Data 3

Function	Pin #	Type	Description
LCD_DATA[3]	31^	O	LCD Interface Data 3
LCD_DATA[3]	67*	O	LCD Interface Data 3
LCD_DATA[4]	70^	O	LCD Interface Data 4
LCD_DATA[4]	6	O	LCD Interface Data
LCD_DATA[4]	61*	O	LCD Interface Data 4
LCD_DATA[5]	66^	O	LCD Interface Data 5
LCD_DATA[5]	32	O	LCD Interface Data 5
LCD_DATA[5]	63*	O	LCD Interface Data 5
LCD_DATA[6]	58^	O	LCD Interface Data 6
LCD_DATA[6]	21	O	LCD Interface Data 6
LCD_DATA[6]	75	O	LCD Interface Data 6
LCD_DATA[7]	50^	O	LCD Interface Data 7
LCD_DATA[7]	19	O	LCD Interface Data 7
LCD_DATA[7]	73	O	LCD Interface Data 7
LCD_DATA[8]	52^	O	LCD Interface Data 8
LCD_DATA[8]	17	O	LCD Interface Data 8
LCD_DATA[8]	51*	O	LCD Interface Data 8
LCD_DATA[9]	68^	O	LCD Interface Data 9
LCD_DATA[9]	8	O	LCD Interface Data 9
LCD_DATA[9]	2	O	LCD Interface Data 9
LCD_ENABLE	75	O	LCD Interface Enable Signal
LCD_ENABLE	42	O	LCD Interface Enable Signal
LCD_ENABLE	4	O	LCD Interface Enable Signal
LCD_HSYNC	74	O	LCD Interface Horizontal Sync
LCD_HSYNC	44	O	LCD Interface Horizontal Sync
LCD_HSYNC	12	O	LCD Interface Horizontal Sync
LCD_RD_E	83*	IO	LCD Interface RD_E Signal
LCD_RESET	36	O	LCD Interface Reset
LCD_RESET	151	O	LCD Interface Reset
LCD_VSYNC	76	O	LCD Interface Vertical Sync
LCD_VSYNC	46	O	LCD Interface Vertical Sync
LCD_VSYNC	14	O	LCD Interface Vertical Sync
LCD_WR_RWN	81*	IO	LCD Interface WR Signal

Notes:
[*]Pins marked with * are connected to iMX7 SoC balls only on specific subsets of SOMs. Otherwise, ball is connected to On SOM devices and pin is used to export devices' interface.
[^] Pins marked with ^ are being latched at boot to determine boot sequence. External drivers to this pin should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see Boot section.

4.1.3 DSI

VAR-SOM-MX7-5G_V2 MIPI DSI Host Controller supports up to 2 D-PHY data lanes.
Key features of the MIPI DSI:

- Maximum resolution ranges up to SXGA+(1400 x 11050 @ 60 Hz, 24 bpp)
  It should be decided on bandwidth between input clock (video clock) and output clock (D-PHY HS clock).

- Supports 1, 2 data lanes
- Supports pixel format: 16 bpp, 18 bpp packed, 18 bpp loosely packed (3 byte format), and 24bpp
- Complies with Protocol-to-PHY Interface (PPI) in 1.0 Gbps / 1.5 Gbps MIPI DPHY
- Supports RGB Interface for Video Image Input from general display controller
- Supports S-i80 (Synchronous i80) Interface for Command Mode Image input from display controller
- Supports PMS control interface for PLL to configure byte clock frequency
- Supports Prescaler to generate escape clock from byte clock

DSI signals:

Signal	Pin #	Type	Description
MIPI_DSI_CLK_N	95	ODS	Negative MIPI DSI clock differential
MIPI_DSI_CLK_P	93	ODS	Positive MIPI DSI clock differential
MIPI_DSI_D0_N	89	ODS	Negative MIPI DSI data 0 differential
MIPI_DSI_D0_P	87	ODS	Positive MIPI DSI data 0 differential
MIPI_DSI_D1_N	101	ODS	Negative MIPI DSI data 1 differential
MIPI_DSI_D1_P	99	ODS	Positive MIPI DSI data 1 differential

5.2. Camera Interfaces

5.2.1. MIPI CSI-2

The CSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between the system and the MIPI D-PHY, allowing communication with an MIPI CSI-2 compliant camera sensor.

The MIPI CSI-2 host controller supports the following features:

- Compliant to MIPI D-phy standard specification V1.1
- Compliant to previous version of Samsung D-phy
- Compliant to MIPI CSI2 Standard Specification V1.01r06
- Support primary and secondary Image format:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - Compressed format: 10-6-10, 10-7-10, 10-8-10, 14-10-14
  - All of user defined byte-based Data packet
- Support embedded byte-based non-Image data packet and generic short packets
- Support interleave mode using Virtual channel
- Support up to two D-PHY Rx Data Lanes
- Interfaces:
  - Compatible to PPI (Protocol-to-PHY Interface) in MIPI D-PHY Specification
  - Image output data bus width: 32 bits (optional)
  - Support four channel virtual channels or data interleave
- Memory:

  Non-image memory:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits

- This memory can store maximum 4 KB of non-image data per frame.

Image Memory:
- 1KB SRAM for image memory
- This memory works as buffering for the difference of input / output bandwidth

- Pixel clock can be gated when no ppi data is coming.

MIPI CSI-2 signals:

Signal	Pin #	Type	Description
MIPI_CSI_CLK_N	88	IDS	Negative MIPI CSI-2 clock differential
MIPI_CSI_CLK_P	86	IDS	Positive MIPI CSI-2 clock differential
MIPI_CSI_D0_N	82	IDS	Negative MIPI CSI-2 data 0 differential
MIPI_CSI_D0_P	80	IDS	Positive MIPI CSI-2 data 0 differential
MIPI_CSI_D1_N	94	IDS	Negative MIPI CSI-2 data 1 differential
MIPI_CSI_D1_P	92	IDS	Positive MIPI CSI-2 data 1 differential

5.2.2. Parallel CSI

The CSI enables the chip to connect directly to external CMOS image sensors.
CMOS image sensors are separated into two classes, dumb and smart.
Dumb sensors are those that support only traditional sensor timing (Vertical SYNC and Horizontal SYNC) and output only Bayer and statistics data, while smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

The capabilities of the CSI include:
- Configurable interface logic to support most commonly available CMOS sensors.
- Support for CCIR656 video interface as well as traditional sensor interface.
- 8-bit / 24-bit data port for YCbCr, YUV, or RGB data input.
- 8-bit / 10-bit / 16-bit data port for Bayer data input.
- Full control of 8-bit/pixel, 10-bit/pixel or 16-bit / pixel data format to 64-bitreceive FIFO packing.
- 256 x 64 FIFO to store received image pixel data.
- Revive FIFO overrun protection mechanism.
- Embedded DMA controllers to transfer data from receive FIFO or statistic FIFO through AHB bus.
- Support 2D DMA transfer from the receive FIFO to the frame buffers in the external memory.
- Single interrupt source to interrupt controller from maskable interrupt sources: Start of Frame, End of Frame, Change of Field, FIFO full, FIFO overrun, DMA transfer done, CCIR error and AHB bus response error.
- Configurable master clock frequency output to sensor.
- Statistic data generation for Auto Exposure (AE) and Auto White Balance (AWB) control of the camera (only for Bayer data and 8-bit/pixel format).
- Supports simple deinterlacing of interlaced input.

Parallel CSI Signals:

Signal	Pin #	Type	Description
CSI1_DATA[0]	38^	I	Parallel Camera Data bit 0
CSI1_DATA[1]	29^	I	Parallel Camera Data bit 1
CSI1_DATA[10]	26	I	Parallel Camera Data bit 10
CSI1_DATA[11]	20	I	Parallel Camera Data bit 11
CSI1_DATA[12]	22	I	Parallel Camera Data bit 12
CSI1_DATA[13]	30	I	Parallel Camera Data bit 13
CSI1_DATA[14]	28^	I	Parallel Camera Data bit 14
CSI1_DATA[15]	33^	I	Parallel Camera Data bit 15
CSI1_DATA[16]	48	I	Parallel Camera Data bit 16
CSI1_DATA[17]	42	I	Parallel Camera Data bit 17
CSI1_DATA[18]	44	I	Parallel Camera Data bit 18
CSI1_DATA[19]	46	I	Parallel Camera Data bit 19
CSI1_DATA[2]	60^	I	Parallel Camera Data bit 2
CSI1_DATA[20]	40^	I	Parallel Camera Data bit 2
CSI1_DATA[21]	23^	I	Parallel Camera Data bit 20
CSI1_DATA[22]	27^	I	Parallel Camera Data bit 21
CSI1_DATA[23]	31^	I	Parallel Camera Data bit 22
CSI1_DATA[3]	72^	I	Parallel Camera Data bit 23
CSI1_DATA[4]	62^	I	Parallel Camera Data bit 3
CSI1_DATA[5]	56^	I	Parallel Camera Data bit 3
CSI1_DATA[6]	54^	I	Parallel Camera Data bit 4
CSI1_DATA[6]	153	I	Parallel Camera Data bit 4
CSI1_DATA[7]	64^	I	Parallel Camera Data bit 5
CSI1_DATA[7]	149	I	Parallel Camera Data bit 5
CSI1_DATA[8]	68^	I	Parallel Camera Data bit 6
CSI1_DATA[8]	147	I	Parallel Camera Data bit 6
CSI1_DATA[9]	52^	I	Parallel Camera Data bit 7
CSI1_DATA[9]	151	I	Parallel Camera Data bit 7
CSI1_FIELD	36	I	Parallel Camera Data bit 8
CSI1_HSYNC	66	I	Parallel Camera Data bit 8
CSI1_HSYNC	155	I	Parallel Camera Data bit 9
CSI1_MCLK	50^	O	Parallel Camera Data bit 9
CSI1_MCLK	173	O	Parallel Camera Field
CSI1_PIXCLK	58^	I	Parallel Camera Horizontal Sync
CSI1_PIXCLK	175	I	Parallel Camera Horizontal Sync
CSI1_VSYNC	70^	I	Parallel Camera Master clock
CSI1_VSYNC	157	I	Parallel Camera Master clock

Note:

[^] Pins marked with ^ are being latched at boot to determine boot sequence. External drivers to this pin should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see Boot section.

5.3. Resistive Touch

The VAR-SOM-MX7-5G_V2 features a 4-wire resistive touch panel interface.

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

Resistive Touch Controller Signals:

Signal	Pin #	Type	Description
TS_X-	39	AI	Touch screen X minus
TS_Y-	41	AI	Touch screen Y minus
TS_X+	35	AI	Touch screen X plus
TS_Y+	37	AI	Touch screen Y plus

5.4. Analog to Digital Converter

The iMX7 exposes 2 ADCs with 4 input channels each.
Input range for ADC lines is 0-1.8V with 12-bit ADC for Low-voltage digital interface.

The following summarizes the key features of the ADC:

- Support five conversion pairs, can work simultaneously, with different conversion Priority.
- Word size is 12-bits
- Support Single and Continue conversion.
- Support Compare mode and channel auto disable if data match the requirement.
- Support Average conversion, Support flexible 4, 8, 16, 32 number of conversion data.
- Configurable sample time and conversion speed / power. The ADC core clock can vary from 300 kHz to 6 MHz, and the maximum sample rate is 1/6 ADC core clock.
- Conversion complete, hardware average complete, compare, DMA, time out flag and interrupt.
- Automatic compare with interrupt for less than, greater than, and equal to, within range, or out-of-range, programmable value.

Note: ADC1 Interface is available on SOMs with no Resistive Touch controller assembled.

ADC1 Signals:

Signal	Pin #	Type	Description
ADC1_IN0	41	AI	Analog to Digital Converter 1 channel 0 (1.8V)
ADC1_IN1	37	AI	Analog to Digital Converter 1 channel 1 (1.8V)
ADC1_IN2	39	AI	Analog to Digital Converter 1 channel 2 (1.8V)
ADC1_IN3	35	AI	Analog to Digital Converter 1 channel 3 (1.8V)

ADC2 Signals:

Signal	Pin #	Type	Description
ADC2_IN0	199	AI	Analog to Digital Converter 2 channel 0 (1.8V)
ADC2_IN1	195	AI	Analog to Digital Converter 2 channel 1 (1.8V)
ADC2_IN2	197	AI	Analog to Digital Converter 2 channel 2 (1.8V)
ADC2_IN3	201	AI	Analog to Digital Converter 2 channel 3 (1.8V)

5.5. Gigabit Ethernet

The core implements 2 triple-speed 10/100/1000-Mbit/s Ethernet MACs compliant with the IEEE802.3-2002 standard. The i.MX7 processor also consists of HW support for IEEE1588 standard.
The On SOM dual Gigabit PHY (Texas Instruments DP83867IRRGZ) in conjunction with external magnetics on carrier board complete the interface to the media.

Note: ETH2 Interface is available only on iMX7D based SOMs.

Gigabit Ethernet1 Signals:

Signal	Pin #	Type	Description
ETH1_MDI_A_P	105	DS	Ethernet1 Positive A differential lane
ETH1_MDI_A_M	107	DS	Ethernet1 Negative A differential lane
ETH1_MDI_B_P	111	DS	Ethernet1 Positive B differential lane
ETH1_MDI_B_M	113	DS	Ethernet1 Negative B differential lane
ETH1_MDI_C_P	117	DS	Ethernet1 Positive C differential lane
ETH1_MDI_C_M	119	DS	Ethernet1 Negative C differential lane
ETH1_MDI_D_P	123	DS	Ethernet1 Positive D differential lane
ETH1_MDI_D_M	125	DS	Ethernet1 Negative D differential lane

Gigabit Ethernet2 Signals:

Signal	Pin #	Type	Description
ETH2_MDI_A_P	49	DS	Ethernet2 Positive A differential lane
ETH2_MDI_A_M	51	DS	Ethernet2 Negative A differential lane
ETH2_MDI_B_P	55	DS	Ethernet2 Positive B differential lane
ETH2_MDI_B_M	57	DS	Ethernet2 Negative B differential lane
ETH2_MDI_C_P	61	DS	Ethernet2 Positive C differential lane
ETH2_MDI_C_M	63	DS	Ethernet2 Negative C differential lane
ETH2_MDI_D_P	67	DS	Ethernet2 Positive D differential lane
ETH2_MDI_D_M	69	DS	Ethernet2 Negative D differential lane

TI-DP83867IRRGZ Ethernet PHY LED Behavior

Signal	10M link	10M active	100M link	100M active	1000M link	1000M active
ETHx_LED_LINK_10_100	OFF	OFF	OFF	OFF	OFF	OFF
ETHx_LED_LINK_1000	ON	ON	ON	ON	ON	ON
ETHx_LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

5.6. 10/100/1000-Mbps Ethernet MAC (ENET)

In case the on SOM Ethernet PHYs are not assembled the ENET interface lines are exposed through the SO-DIMM 204 pin connector.

Note: ENET2 Interface is available only on iMX7D based SOMs.

ENET1 Signals:

Signal	Pin #	Type	Description
ENET1_1588_EVENT0_IN	156	I	ENET1 1588 EVENT 0 IN
ENET1_1588_EVENT0_OUT	158	O	ENET1 1588 EVENT 0 OUT
ENET1_1588_EVENT1_IN	152	I	ENET1 1588 EVENT 1 IN
ENET1_1588_EVENT1_OUT	154	O	ENET1 1588 EVENT 1 OUT
ENET1_1588_EVENT2_IN	48	I	ENET1 1588 EVENT 2 IN
ENET1_1588_EVENT2_OUT	30	O	ENET1 1588 EVENT 2 OUT
ENET1_1588_EVENT3_IN	42	I	ENET1 1588 EVENT 3 IN
ENET1_1588_EVENT3_OUT	22	O	ENET1 1588 EVENT 3 OUT
ENET1_COL	15*	I	ENET1 COL
ENET1_CRS	7*	I	ENET1 CRS
ENET1_MDC	185	O	ENET1 MDC
ENET1_MDC	161	O	ENET1 MDC
ENET1_MDC	45~	O	ENET1 MDC
ENET1_MDIO	181	IO	ENET1 MDIO
ENET1_MDIO	159	IO	ENET1 MDIO
ENET1_MDIO	43~	IO	ENET1 MDIO
ENET1_RGMII_RD0	105*	I	ENET1 RGMII receive data 0
ENET1_RGMII_RD1	107*	I	ENET1 RGMII receive data 1
ENET1_RGMII_RD2	111*	I	ENET1 RGMII receive data 2
ENET1_RGMII_RD3	113*	I	ENET1 RGMII receive data 3
ENET1_RGMII_RX_CTL	119*	I	ENET1 RGMII RX_CTL
ENET1_RGMII_RXC	117*	I	ENET1 RGMII RXC
ENET1_RGMII_TD0	123*	O	ENET1 RGMII transmit data 0
ENET1_RGMII_TD1	125*	O	ENET1 RGMII transmit data 1
ENET1_RGMII_TD2	129*	O	ENET1 RGMII transmit data 2
ENET1_RGMII_TD3	133*	O	ENET1 RGMII transmit data 3
ENET1_RGMII_TX_CTL	135*	O	ENET1 RGMII TX_CTL
ENET1_RGMII_TXC	131*	O	ENET1 RGMII TXC
ENET1_RX_CLK	13*	I	ENET1 RX CLK
ENET1_TX_CLK	9*	O	ENET1 TX CLK

ENET2 Signals:

Signal	Pin #	Type	Description
ENET2_1588_EVENT0_IN	159	I	ENET2 1588 EVENT 0 IN
ENET2_1588_EVENT0_OUT	161	O	ENET2 1588 EVENT 0 OUT
ENET2_1588_EVENT2_IN	44	I	ENET2 1588 EVENT 2 IN
ENET2_1588_EVENT2_OUT	20	O	ENET2 1588 EVENT 2 OUT
ENET2_1588_EVENT3_IN	46	I	ENET2 1588 EVENT 3 IN
ENET2_1588_EVENT3_OUT	26	O	ENET2 1588 EVENT 3 OUT
ENET2_COL	76	I	ENET2 COL
ENET2_CRS	74	I	ENET2 CRS
ENET2_MDC	45~	O	ENET2 MDC
ENET2_MDIO	43~	IO	ENET2 MDIO
ENET2_RGMII_RD0	49*	I	ENET2 RGMII receive data 0
ENET2_RGMII_RD1	51*	I	ENET2 RGMII receive data 1
ENET2_RGMII_RD2	55*	I	ENET2 RGMII receive data 2
ENET2_RGMII_RD3	57*	I	ENET2 RGMII receive data 3
ENET2_RGMII_RX_CTL	63*	I	ENET2 RGMII RX_CTL
ENET2_RGMII_RXC	61*	I	ENET2 RGMII RXC
ENET2_RGMII_TD0	67*	O	ENET2 RGMII transmit data 0
ENET2_RGMII_TD1	69*	O	ENET2 RGMII transmit data 1
ENET2_RGMII_TD2	77*	O	ENET2 RGMII transmit data 2
ENET2_RGMII_TD3	81*	O	ENET2 RGMII transmit data 3
ENET2_RGMII_TX_CTL	83*	O	ENET2 RGMII TX_CTL
ENET2_RGMII_TXC	79*	O	ENET2 RGMII TXC
ENET2_RX_CLK	75	I	ENET2 RX CLK
ENET2_TX_CLK	73	O	ENET2 TX CLK

Note:
[*]Pins marked with * are connected to iMX7 SoC balls only on specific subsets of SOMs. Otherwise, ball is connected to On SOM devices and pin is used to export devices' interface.
[~] Pins marked with ~ are used by certain subsets of SOMs for internal SOM connections, Pin function must not be altered if using these subsets.

5.7. Wi-Fi & Bluetooth

The VAR-SOM-MX7-5G_V2 contains a certified high performance Wi-Fi and Bluetooth module.
it supports IEEE 802.11 ac/a/b/g/n/ax + Bluetooth 5.4 BR/EDR/LE.

The modules have an antenna connection through a U.FL JACK connector.
Antenna cable connected to module must have 50-Ω impedance.
In order to give the most flexible solution the Bluetooth UART and Bluetooth Audio bus is buffered and it can be disconnected from the module and used by external circuity.

One of the following options can be implemented:

- The system will use all the wireless interfaces: Wi-Fi, Bluetooth, and Bluetooth Audio.
  In this case all the external pins of the interfaces should be left floating.
  (not default assembly, module should be purchased with Bluetooth Audio assembled)
- The system will use the following wireless interfaces: Wi-Fi, Bluetooth.
  In this case all the external pins of the interfaces should be left floating.
  Bluetooth Audio is available for use

(default assembly).

- The system will use only Wi-Fi; the Bluetooth interface will not be used. In this case The Bluetooth should be disabled, and Bluetooth buffer should be disabled. The Bluetooth module pins will be entering Hi-Z and the SOC pins will be accessible.
- The system will not use wireless connections. In this case the module can be purchased without Wi-Fi module assembled and all the interfaces are accessible.

Bluetooth Interface signals:

Signal	Pin #	Type	Description
SAI2_TX_SYNC	179	IO	Bluetooth Audio Frame Sync
SAI2_RX_DATA	174	I	Bluetooth Audio RX Data
SAI2_TX_BCLK	177	IO	Bluetooth Audio TX Byte Clock
SAI2_TX_DATA	178	O	Bluetooth Audio TX Data
BT_UART_CTS_B	154	O	Bluetooth UART CTS
BT_UART_RTS_B	152	I	Bluetooth UART RTS
BT_UART_RX	156	I	Bluetooth UART RX
BT_UART_TX	158	O	Bluetooth UART TX

5.8. USB Ports

The USB controller block provides high performance USB functionality that conforms to the Universal Serial Bus Specification, Rev. 2.0 (Compaq, Hewlett-Packard, Intel, Lucent, Microsoft, NEC, Philips; 2000), and the On-The-Go and Embedded Host Supplement to the USB Revision2.0 Specification (Hewlett-Packard Company, Intel Corporation, LSI Corporation, Microsoft Corporation, Renesas Electronics Corporation, ST-Ericsson; 2012).
The USB controller consists of three independent USB controller cores: two On-The-Go (OTG) controller cores, and one Host-only controller core. Each controller core connects to its dedicated on-chip USB PHY instance using a UTMI interface.
See i.MX 7Dual Applications Processor Reference Manual for more details.
All three controller cores are single-port cores.

5.8.1. USB OTG Cores

The VAR-SOM-MX7-5G_V2 supports USB_OTG1 as True OTG port interface and USB_OTG2 as USB Host Port.

Note: USB_OTG2 Port is available only on iMX7D based SOMs.

USB OTG Signals:

Signal	Pin #	Type	Description
USB_OTG1_DN	108	IODS	Negative USB OTG data
USB_OTG1_DP	106	IODS	Positive USB OTG data
USB_OTG1_VBUS	110	I	USB 2.0 OTG VBUS (5V)
USB_OTG1_ID	104	I	USB OTG host/client ID Low : Host mode Float: Client mode

USB Host Signals:

Signal	Pin #	Type	Description
USB_OTG2_DN	100	IODS	Negative USB Host data
USB_OTG2_DP	98	IODS	Positive USB Host data
USB_OTG2_VBUS	102	I	USB 2.0 VBUS (5V)

5.8.2. HSIC USB

HSIC USB Signals:

Signal	Pin #	Type	Description
HSIC_DATA	112	IODS	high-speed inter-chip USB data
HSIC_STROBE	114	IODS	high-speed inter-chip USB strobe

5.9. MMC/SD/SDIO

Key VAR-SOM-MX7-5G_V2 MMC interface features:

- Conforms to the SD Host Controller Standard Specification version 3.0
- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.41/4.5/5.0
- Compatible with the SD Memory Card Specification version 2.0 and supports the Extended Capacity SD Memory Card
- Compatible with the SDIO Card Specification version 2.0

- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit MMC modes up to 25MB/s HS mode

(25MB/s max)SDMMC2 Signals:

Signal	Pin #	Type	Description
SD1_CLK	128	O	SD Card 1 Interface Clock Signal
SD1_CMD	122	O	SD Card 1 Interface Command Signal
SD1_DATA0	132	IO	SD Card 1 Interface Data 0 Signal
SD1_DATA1	126	IO	SD Card 1 Interface Data 1 Signal
SD1_DATA2	124	IO	SD Card 1 Interface Data 2 Signal
SD1_DATA3	130	IO	SD Card 1 Interface Data 3 Signal

5.10. Audio

The VAR-SOM-MX7-5G_V2 features three audio interfaces:

- WM8731 Audio codec Analog outputs / input interfaces:
  - stereo line-in
  - Stereo HP out
  - Mono microphone input
- Serial audio interface (SAI)
- Medium quality sound (MQS)

Analog audio signals are featured by the on-SOM WM8731 audio codec. Refer to the data sheet for detailed electrical characteristics of the relevant interfaces http://www.cirrus.com/en/pubs/proDatasheet/WM8731_v4.9.pdf

Analog Audio Signals:

Signal	Pin #	Type	Description
MICBIAS	1*	AP	Microphone Bias
MICIN	3	AI	Microphone In
AGND	5	AP	Audio Interface Ground Reference
RLINEIN	7*	AI	Line-in - Right
LLINEIN	9*	AI	Line-in - Left
AGND	11	AP	Audio Interface Ground Reference
HPROUT	13*	AO	Headphones out - right
HPLOUT	15*	AO	Headphones out - left

Note:
[*]Pins marked with * are connected to iMX7 SoC balls only on specific subsets of SOMs. Otherwise, ball is connected to On SOM devices and pin is used to export devices' interface.

Synchronous Audio Interface (SAI)

The synchronous audio interface (SAI) supports full-duplex serial interfaces with frame Synchronization such as I2S, AC97, TDM, and codec/DSP interfaces.

SAI Interface features:

- Transmitter with independent Bit Clock and Frame Sync supporting 1 data line
- Receiver with independent Bit Clock and Frame Sync supporting 1 data line
- Maximum Frame Size of 32 Words
- Word size programmable from 8-bits to 32-bits
- Word size configured separately for first word and remaining words in frame.
- Asynchronous FIFO for each Transmit and Receive data line
- Graceful restart after FIFO Error

The SOM can export up to 3 Synchronous Audio Interfaces.

Note:

SAI1 is used internally by audio codec and is available on SOM modules with no Audio codec assembled.
SAI2 is used by Bluetooth Audio. It is available on SOM modules with no Bluetooth Audio support.

Synchronous Audio Signals:

Signal	Pin #	Type	Description
SAI1_MCLK	1*	IO	Serial Audio Interface 1 Master Clock
SAI1_RX_BCLK	172	IO	Serial Audio Interface 1 RX Byte Clock
SAI1_RX_BCLK	131*	IO	Serial Audio Interface 1 RX Byte Clock
SAI1_RX_DATA[0]	9*	I	Serial Audio Interface 1 RX Data
SAI1_RX_SYNC	176	IO	Serial Audio Interface 1 RX Sync
SAI1_RX_SYNC	135*	IO	Serial Audio Interface 1 RX Sync
SAI1_TX_BCLK	13*	IO	Serial Audio Interface 1 TX Byte Clock
SAI1_TX_DATA[0]	15*	O	Serial Audio Interface 1 TX Data
SAI1_TX_SYNC	7*	IO	Serial Audio Interface 1 TX Sync
SAI2_MCLK	168	IO	Serial Audio Interface 2 Master Clock
SAI2_RX_BCLK	172	IO	Serial Audio Interface 2 RX Byte Clock
SAI2_RX_DATA[0]	174	I	Serial Audio Interface 2 RX Data
SAI2_RX_SYNC	176	IO	Serial Audio Interface 2 RX Sync
SAI2_TX_BCLK	177	IO	Serial Audio Interface 2 TX Byte Clock
SAI2_TX_DATA[0]	178	O	Serial Audio Interface 2 TX Data
SAI2_TX_SYNC	179	IO	Serial Audio Interface 2 TX Sync
SAI3_MCLK	161	IO	Serial Audio Interface 3 Master Clock
SAI3_MCLK	187~	IO	Serial Audio Interface 3 Master Clock
SAI3_RX_BCLK	122	IO	Serial Audio Interface 3 RX Byte Clock
SAI3_RX_DATA[0]	132	I	Serial Audio Interface 3 RX Data
SAI3_RX_SYNC	156	IO	Serial Audio Interface 3 RX Sync
SAI3_RX_SYNC	128	IO	Serial Audio Interface 3 RX Sync
SAI3_TX_BCLK	158	IO	Serial Audio Interface 3 TX Byte Clock
SAI3_TX_BCLK	126	IO	Serial Audio Interface 3 TX Byte Clock
SAI3_TX_DATA[0]	152	O	Serial Audio Interface 3 TX Data
SAI3_TX_DATA[0]	130	O	Serial Audio Interface 3 TX Data
SAI3_TX_SYNC	154	IO	Serial Audio Interface 3 TX Sync
SAI3_TX_SYNC	124	IO	Serial Audio Interface 3 TX Sync

[*]Pins marked with * are connected to iMX7 SoC balls only on specific subsets of SOMs. Otherwise, ball is connected to On SOM devices and pin is used to export devices' interface.
[~] Pins marked with ~ are used by certain subsets of SOMs for internal SOM connections, Pin function must not be altered if using these subsets.

Medium quality sound (MQS):

Medium quality sound (MQS) is used to generate medium quality audio via a standard GPIO in the pinmux, allowing the user to connect stereo speakers or headphones to a power amplifier without an additional DAC chip. MQS provides only simple audio reproduction. No internal pop, click or distortion artifact reduction methods are provided.

MQS Signals:

Signal	Pin #	Type	Description
MQS_RIGHT	176	O	Right signal output
MQS_LEFT	172	O	Left signal output

5.11. PCIe

VAR-SOM-MX7-5G_V2 PCI Exports the PCIe interface which supports 6.0 Gbps data rate and complies to PCI Express base specification 2.1.

PCI PHY Key features:

- 1.5 / 2.5 / 3.0 / 5.0 / 6.0 Gbps Serializer / Deserializer
- Compliant with PCI Express Base Specification 2.1
- Compliant with PIPE Specification 2.0
- 8 / 16 / 20 / 40-bit CMOS Interface for Transmitter and Receiver
- 25 / 100 MHz Reference Clock
- K28.5 Detection for Word Alignment
- 8B/10B Encoding / Decoding
- Receiver Detection
- 28 nm CMOS Process (LN28LPP)
- Supports Spread Spectrum Clocking in Transmitter and Receiver

Note: PCIe Interface is available only on iMX7D based SOMs.

PCIE Signals:

Signal	Pin #	Type	Description
PCIE_TX_P	182	DSO	Positive PCIe differential output
PCIE_TX_N	184	DSO	Negative PCIe differential output
PCIE_REFCLK_P	188	DSI	Positive Reference Clock Differential Input for PCIe
PCIE_REFCLK_N	190	DSI	Negative Reference Clock Differential Input for PCIe
PCIE_REFCLKOUT_P	194	DSO	Positive Reference Clock Differential Output for PCIe
PCIE_REFCLKOUT_N	196	DSO	Negative Reference Clock Differential Output for PCIe
PCIE_RX_P	200	DSI	Positive PCIe differential input
PCIE_RX_N	202	DSI	Negative PCIe differential input

5.12. Flexible Controller Area Network (FLEXCAN)

The VAR-SOM-MX7-5G_V2 Exposes 2 FLEXCAN interfaces.
The Flexible Controller Area Network (FLEXCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The CAN protocol was primarily designed to be used as a vehicle serial data bus meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN module is a full implementation of the CAN protocol specification, which supports both standard and extended message frames. 64 Message Buffers are supported.

CAN1 Signals:

Signal	Pin #	Type	Description
CAN1_TX	120	O	CAN BUS transmit
CAN1_TX	113*	O	CAN BUS transmit
CAN1_RX	183	I	CAN BUS receive
CAN1_RX	111*	I	CAN BUS receive
CAN2_TX	155	O	CAN BUS transmit

CAN2 Signals:

Signal	Pin #	Type	Description
CAN2_TX	133*	O	CAN BUS transmit
CAN2_RX	157	I	CAN BUS receive
CAN2_RX	129*	I	CAN BUS receive

Signal Descriptions
CAN Rx: The receive pin from the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.
CAN Tx: The transmit pin to the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.

[*] Pins marked with * are connected to iMX7 SoC balls only on specific subsets of SOMs. Otherwise, ball is connected to On SOM devices and pin is used to export devices' interface.

5.13. UART Interfaces

The VAR-SOM-MX7-5G_V2 exposes up to 7 UART interfaces some of which are muxed with other peripherals. UART3 is used on SOM for Bluetooth interface and can be accessible only in when Bluetooth interface is not in use.

Universal Asynchronous Receiver/Transmitter (UART) provides serial communication capability with external devices through a level converter and an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low speed IrDA compatibility. UART supports NRZ encoding format, RS485 compatible 9 bit data format and IrDA compatible infrared slow data rate (SIR) format.

UART1 Signals:

Signal	Pin #	Type	Description
UART1_TXD	161	O	UART transmit
UART1_TXD	113*	O	UART transmit
UART1_RXD	159	I	UART receive
UART1_RXD	111*	I	UART receive
UART1_RTS	177	I	UART HW flow control RTS
UART1_RTS	107*	I	UART HW flow control RTS
UART1_CTS	179	O	UART HW flow control CTS
UART1_CTS	105*	O	UART HW flow control CTS

Note:
[*] Pins marked with * are connected to iMX7 SoC balls only on specific subsets of SOMs. Otherwise, ball is connected to On SOM devices and pin is used to export devices' interface.

UART2 Signals:

Signal	Pin #	Type	Description
UART2_TXD	42	O	UART transmit
UART2_RXD	48	I	UART receive
UART2_RTS	44	I	UART HW flow control RTS
UART2_RTS	178	I	UART HW flow control RTS
UART2_CTS	46	O	UART HW flow control CTS
UART2_CTS	174	O	UART HW flow control CTS

UART3 Signals:

Signal	Pin #	Type	Description
UART3_TXD	183	O	UART transmit
UART3_TXD	158	O	UART transmit
UART3_RXD	156	I	UART receive
UART3_RTS	181	I	UART HW flow control RTS
UART3_RTS	152	I	UART HW flow control RTS
UART3_CTS	185	O	UART HW flow control CTS
UART3_CTS	154	O	UART HW flow control CTS

UART4 Signals:

Signal	Pin #	Type	Description
UART4_TXD	171~	O	UART transmit
UART4_TXD	177	O	UART transmit
UART4_RXD	169~	I	UART receive
UART4_RXD	179	I	UART receive
UART4_RTS	167	I	UART HW flow control RTS
UART4_RTS	178	I	UART HW flow control RTS
UART4_CTS	174	O	UART HW flow control CTS

UART5 Signals:

Signal	Pin #	Type	Description
UART5_TXD	189	O	UART transmit
UART5_TXD	173	O	UART transmit
UART5_RXD	175	I	UART receive
UART5_RTS	191	I	UART HW flow control RTS
UART5_RTS	155	I	UART HW flow control RTS
UART5_CTS	157	O	UART HW flow control CTS

UART6 Signals:

Signal	Pin #	Type	Description
UART6_TXD	8	O	UART transmit
UART6_TXD	163	O	UART transmit
UART6_RXD	17	I	UART receive
UART6_RXD	118	I	UART receive
UART6_RTS	2	I	UART HW flow control RTS
UART6_CTS	18	O	UART HW flow control CTS
UART6_CTS	128	O	UART HW flow control CTS

UART7 Signals:

Signal	Pin #	Type	Description
UART7_TXD	34	O	UART transmit
UART7_TXD	149	O	UART transmit
UART7_TXD	126	O	UART transmit
UART7_RXD	25	I	UART receive
UART7_RXD	153	I	UART receive
UART7_RXD	132	I	UART receive
UART7_RTS	24	I	UART HW flow control RTS
UART7_RTS	147	I	UART HW flow control RTS
UART7_RTS	130	I	UART HW flow control RTS
UART7_CTS	10	O	UART HW flow control CTS
UART7_CTS	151	O	UART HW flow control CTS
UART7_CTS	124	O	UART HW flow control CTS

[~] Pins marked with ~ are used by certain subsets of SOMs for internal SOM connections, Pin function must not be altered if using these subsets.

5.14. Enhanced Configurable SPI (ECSPI)

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, synchronous 4-wire serial communication block. The ECSPI contains a 64 x 32 receive buffer (RXFIFO) and a 64 x 32 transmit buffer (TXFIFO). With data FIFOs, the ECSPI allows rapid data communication with fewer software interruptions.

ECSPI Key Features:

- Full-duplex synchronous serial interface
- Master/slave configurable
- Four chip select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmitting and receiving data
- Polarity and phase of the chip select (SS) and SPI clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Max operation frequency up to the reference clock frequency

Note: ECSPI1 is used by on SOM Resistive touch controller. It can be used externally only if ECSPI1 is not used by Resistive touch controller.

ECSPI1 Signals:

Signal	Pin #	Type	Description
ECSPI1_MISO	156	IO	ECSPI 1 Master In Slave Out
ECSPI1_MOSI	158	IO	ECSPI 1 Master Out Slave In
ECSPI1_SCLK	152	IO	ECSPI 1 Clock
ECSPI1_SS0	154	IO	ECSPI 1 Chip Select 0
ECSPI1_SS1	159	IO	ECSPI 1 Chip Select 1
ECSPI1_SS2	161	IO	ECSPI 1 Chip Select 2
ECSPI1_TESTER_ TRIGGER	113*	IO	ECSPI 1 Tester Trigger

ECSPI2 Signals:

Signal	Pin #	Type	Description
ECSPI2_MISO	147	IO	ECSPI 2 Master In Slave Out
ECSPI2_MISO	129*	IO	ECSPI 2 Master In Slave Out
ECSPI2_MOSI	149	IO	ECSPI 2 Master Out Slave In
ECSPI2_MOSI	113*	IO	ECSPI 2 Master Out Slave In
ECSPI2_RDY	125*	I	ECSPI 2 Ready
ECSPI2_SCLK	111*	IO	ECSPI 2 Clock
ECSPI2_SCLK	153	IO	ECSPI 2 Clock
ECSPI2_SS0	151	IO	ECSPI 2 Chip Select 0
ECSPI2_SS0	133*	IO	ECSPI 2 Chip Select 0
ECSPI2_SS1	119*	IO	ECSPI 2 Chip Select 1
ECSPI2_SS2	117*	IO	ECSPI 2 Chip Select 2
ECSPI2_SS3	123*	IO	ECSPI 2 Chip Select 3

ECSPI3 Signals:

Signal	Pin #	Type	Description
ECSPI3_MISO	179	IO	ECSPI 3 Master In Slave Out
ECSPI3_MOSI	177	IO	ECSPI 3 Master Out Slave In
ECSPI3_SCLK	169~	IO	ECSPI 3 Clock
ECSPI3_SCLK	174	IO	ECSPI 3 Clock
ECSPI3_SS0	171~	IO	ECSPI 3 Chip Select 0
ECSPI3_SS0	178	IO	ECSPI 3 Chip Select 0
ECSPI3_SS1	130	IO	ECSPI 3 Chip Select 1
ECSPI3_SS2	43~	IO	ECSPI 3 Chip Select 2
ECSPI3_SS3	45~	IO	ECSPI 3 Chip Select 3
ECSPI3_TESTER_ TRIGGER	117*	IO	ECSPI 3 Tester Trigger

ECSPI4 Signals:

Signal	Pin #	Type	Description
ECSPI4_MISO	48	IO	ECSPI 4 Master In Slave Out
ECSPI4_MISO	118	IO	ECSPI 4 Master In Slave Out
ECSPI4_MOSI	42	IO	ECSPI 4 Master Out Slave In
ECSPI4_MOSI	163	IO	ECSPI 4 Master Out Slave In
ECSPI4_RDY	124	I	ECSPI 4 Ready
ECSPI4_SCLK	44	IO	ECSPI 4 Clock
ECSPI4_SS0	46	IO	ECSPI 4 Chip Select 0
ECSPI4_SS0	128	IO	ECSPI 4 Chip Select 0
ECSPI4_SS1	122	IO	ECSPI 4 Chip Select 1
ECSPI4_SS2	132	IO	ECSPI 4 Chip Select 2
ECSPI4_SS3	126	IO	ECSPI 4 Chip Select 3
ECSPI4_ TESTER_ TRIGGER	123*	IO	ECSPI 4 Tester Trigger

Note:

[*] Pins marked with * are connected to iMX7 SoC balls only on specific subsets of SOMs. Otherwise, ball is connected to On SOM devices and pin is used to export devices' interface.

[~] Pins marked with ~ are used by certain subsets of SOMs for internal SOM connections, Pin function must not be altered if using these subsets.

5.15. Quad Serial Peripheral Interface (QuadSPI)

The Quad Serial Peripheral Interface (QuadSPI) block acts as an interface to one or two external serial flash devices, each with up to four bidirectional data lines.

QSPI Key Features:

- Flexible sequence engine to support various flash vendor devices.
- Single, dual, quad mode of operation.
- DDR/DTR mode wherein the data is generated on every edge of the serial flash clock.
- Support for flash data strobe signal for data sampling in DDR and SDR mode.
- Two identical serial flash devices can be connected and accessed in parallel for data read operations, forming one (virtual) flash memory with doubled readout bandwidth.
- DMA support
- Multi master accesses with priority
- Memory mapped read access to connected flash devices.
- Programmable sequence engine to cater to future command/protocol changes and able to support all existing vendor commands and operations.
- Supports 3-byte and 4-byte addressing.
  - TXFIFO size is 512Byte
  - RXFIFO size is 512Byte
  - AHB BUF size is 1KByte

QSPI1 Signals:

Signal	Pin #	Type	Description
QSPI_A_DATA[0]	16	IO	I/O data signal 1 port 0 for serial flash device A
QSPI_A_DATA[1]	4	IO	I/O data signal 1 port 1 for serial flash device A
QSPI_A_DATA[2]	14	IO	I/O data signal 1 port 2 for serial flash device A
QSPI_A_DATA[3]	12	IO	I/O data signal 1 port 3 for serial flash device A
QSPI_A_DQS	6	I	Data strobe signal 1 to serial flash device A
QSPI_A_SCLK	32	O	Serial clock output 1 to serial flash device A
QSPI_A_SS0_B	21	O	Chip select 1 port 0 for serial flash device A
QSPI_A_SS1_B	19	O	Chip select 1 port 1 for serial flash device A

QSPI2 Signals:

Signal	Pin #	Type	Description
QSPI_B_DATA[0]	17	IO	I/O data signal 1 port 0 for serial flash device B
QSPI_B_DATA[1]	8	IO	I/O data signal 1 port 1 for serial flash device B
QSPI_B_DATA[2]	2	IO	I/O data signal 1 port 2 for serial flash device B
QSPI_B_DATA[3]	18	IO	I/O data signal 1 port 3 for serial flash device B
QSPI_B_DQS	25	I	Data strobe signal 1 to serial flash device B
QSPI_B_SCLK	34	O	Serial clock output 1 to serial flash device B
QSPI_B_SS0_B	24	O	Chip select 1 port 0 for serial flash device B
QSPI_B_SS1_B	10	O	Chip select 1 port 1 for serial flash device B

5.16. I²C

The VAR-SOM-MX7-5G_V2 SOM exposes up to 4 I2C interfaces on the SOM-DIMM 204 pin connector. I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development. Data rates of up to 400 kbps are supported.

I2C1 Signals:

Signal	Pin #	Type	Description
I2C1_SCL	165	IO	I2C1 I²C clock, open drain
I2C1_SDA	167	IO	I2C1 I²C data, open drain

Note:
[1] I2C1 Interface exported on pins 165,167 is used by On SOM PMIC (address 0x08) and EEPROM (address 0x50 & 0x51) and - Do not alter pins' mode otherwise SOM will not boot.
[2]10K Ohm Pull up resistors on SOM are present for I2C1 interface on SOM.

I2C2 Signals:

Signal	Pin #	Type	Description
I2C2_SCL	169~	IO	I2C2 I²C clock, open drain
I2C2_SDA	171~	IO	I2C2 I²C data, open drain

Note:
[1] I2C2 Interface exported on pins 169,171 is used by Audio codec (address 0x1A) - Do not alter pins' mode otherwise on SOM Audio codec will not work.
[2] 10K Ohm Pull up resistors on SOM are present for I2C2 interface.

I2C3 Signals:

Signal	Pin #	Type	Description
I2C3_SCL	30	IO	I2C3 I²C clock, open drain
I2C3_SCL	157	IO	I2C3 I²C clock, open drain
I2C3_SCL	105*	IO	I2C3 I²C clock, open drain
I2C3_SDA	22	IO	I2C3 I²C data, open drain
I2C3_SDA	155	IO	I2C3 I²C data, open drain
I2C3_SDA	107*	IO	I2C3 I²C data, open drain

Note:
[1] Pull up resistors for I2C3 are NOT available on SOM and should be placed on customboard.
[*] Pins marked with * are connected to iMX7 SoC balls only on specific subsets of SOMs. Otherwise, ball is connected to On SOM devices and pin is used to export devices' interface.

I2C4 Signals:

Signal	Pin #	Type	Description
I2C4_SCL	181	IO	I2C4 I²C clock, open drain
I2C4_SCL	20	IO	I2C4 I²C clock, open drain
I2C4_SCL	175	IO	I2C4 I²C clock, open drain
I2C4_SCL	176	IO	I2C4 I²C clock, open drain
I2C4_SCL	129*	IO	I2C4 I²C clock, open drain
I2C4_SDA	185	IO	I2C4 I²C data, open drain
I2C4_SDA	26	IO	I2C4 I²C data, open drain
I2C4_SDA	173	IO	I2C4 I²C data, open drain
I2C4_SDA	172	IO	I2C4 I²C data, open drain
I2C4_SDA	133*	IO	I2C4 I²C data, open drain

Note:

[1] Pull up resistors for I2C4 are NOT available on SOM and should be placed on customboard.

[*] Pins marked with * are connected to iMX7 SoC balls only on specific subsets of SOMs. Otherwise, ball is connected to On SOM devices and pin is used to export devices' interface.

5.17. Subscriber Identification Module (SIM)

The Subscriber Identification Module (SIM) is designed to facilitate communication to SIM cards or Eurochip pre-paid phone cards, and compatible with ISO/IEC 7816-3 standards. The SIM module has one port that can be used to interface with the various cards.

SIM1 Signals:

Signal	Pin #	Type	Description
SIM1_PORT1_CLK	8	O	Output Clock from the chip to the SmartCard on Port1
SIM1_PORT1_PD	25	I	SmartCard insertion detect for Port1
SIM1_PORT1_RST_B	2	O	SmartCard Reset signal for Port1
SIM1_PORT1_SVEN	18	O	SmartCard power supply enable control signal for Port1
SIM1_PORT1_TRXD	17	O	Transmit/Receive Data signal for Port1
SIM1_PORT2_CLK	4	O	Output Clock from the chip to the SmartCard on Port2
SIM1_PORT2_PD	6	I	SmartCard insertion detect for Port2
SIM1_PORT2_RST_B	14	O	SmartCard Reset signal for Port2
SIM1_PORT2_SVEN	12	O	SmartCard power supply enable control signal for Port2
SIM1_PORT2_TRXD	16	O	Transmit/Receive Data signal for Port2

SIM2 Signals:

Signal	Pin #	Type	Description
SIM2_PORT1_CLK	24	O	Output Clock from the chip to the SmartCard on Port1
SIM2_PORT1_PD	69*	I	SmartCard insertion detect for Port1
SIM2_PORT1_RST_B	10	O	SmartCard Reset signal for Port1
SIM2_PORT1_SVEN	67*	O	SmartCard power supply enable control signal for Port1
SIM2_PORT1_TRXD	34	O	Transmit/Receive Data signal for Port1
SIM2_PORT2_CLK	21	O	Output Clock from the chip to the SmartCard on Port2
SIM2_PORT2_PD	51*	I	SmartCard insertion detect for Port2
SIM2_PORT2_RST_B	19	O	SmartCard Reset signal for Port2
SIM2_PORT2_SVEN	49*	O	SmartCard power supply enable control signal for Port2
SIM2_PORT2_TRXD	32	O	Transmit/Receive Data signal for Port2

Note:

[*] Pins marked with * are connected to iMX7 SoC balls only on specific subsets of SOMs. Otherwise, ball is connected to On SOM devices and pin is used to export devices' interface.

5.18. External Interface Module (EIM)

The EIM handles the interface to devices external to the chip, including generation of chip selects, clock and control for external peripherals and memory. It provides asynchronous access to devices with SRAM-like interface and synchronous access to devices with NOR-Flash-like or PSRAM-like interface.
Please refer to i.MX 7Dual Applications Processor Reference Manual for more information.

EIM Signals:

Signal	Pin #	Type	Description
WEIM_ACLK_FREERUN	38^	I	AXI clock signaL
WEIM_AD[0]	16	IO	LSB multiplexed Address/Data Bus signal
WEIM_AD[1]	4	IO	LSB multiplexed Address/Data Bus signal
WEIM_AD[10]	49*	IO	LSB multiplexed Address/Data Bus signal
WEIM_AD[11]	51*	IO	LSB multiplexed Address/Data Bus signal
WEIM_AD[12]	55*	IO	LSB multiplexed Address/Data Bus signal
WEIM_AD[13]	57*	IO	LSB multiplexed Address/Data Bus signal
WEIM_AD[14]	63*	IO	LSB multiplexed Address/Data Bus signal
WEIM_AD[15]	61*	IO	LSB multiplexed Address/Data Bus signal
WEIM_AD[2]	14	IO	LSB multiplexed Address/Data Bus signal
WEIM_AD[3]	12	IO	LSB multiplexed Address/Data Bus signal
WEIM_AD[4]	6	IO	LSB multiplexed Address/Data Bus signal
WEIM_AD[5]	32	IO	LSB multiplexed Address/Data Bus signal
WEIM_AD[6]	21	IO	LSB multiplexed Address/Data Bus signal
WEIM_AD[7]	19	IO	LSB multiplexed Address/Data Bus signal
WEIM_AD[8]	75	IO	LSB multiplexed Address/Data Bus signal
WEIM_AD[9]	74	IO	LSB multiplexed Address/Data Bus signal
WEIM_ADDR[16]	67*	O	MSB Address Bus signal
WEIM_ADDR[17]	69*	O	MSB Address Bus signal
WEIM_ADDR[18]	77*	O	MSB Address Bus signal
WEIM_ADDR[19]	81*	O	MSB Address Bus signal
WEIM_ADDR[20]	83*	O	MSB Address Bus signal
WEIM_ADDR[21]	79*	O	MSB Address Bus signal
WEIM_ADDR[22]	73	O	MSB Address Bus signal
WEIM_ADDR[23]	30	O	MSB Address Bus signal
WEIM_ADDR[24]	22	O	MSB Address Bus signal
WEIM_ADDR[25]	20	O	MSB Address Bus signal
WEIM_ADDR[26]	26	O	MSB Address Bus signal
WEIM_BCLK	18^	O	Burst Clock signal
WEIM_CRE	29	O	CRE/PS for Cellular Ram memory
WEIM_CS0_B	2	O	Chip Select signal
WEIM_CS1_B	10	O	Chip Select signal
WEIM_CS2_B	33^	O	Chip Select signal
WEIM_CS3_B	28^	O	Chip Select signal
WEIM_DATA[0]	40^	IO	MSB Data Bus signal
WEIM_DATA[1]	23^	IO	MSB Data Bus signal
WEIM_DATA[10]	64^	IO	MSB Data Bus signal
WEIM_DATA[11]	54^	IO	MSB Data Bus signal
WEIM_DATA[12]	56^	IO	MSB Data Bus signal
WEIM_DATA[13]	62^	IO	MSB Data Bus signal
WEIM_DATA[14]	72^	IO	MSB Data Bus signal
WEIM_DATA[15]	60^	IO	MSB Data Bus signal
WEIM_DATA[2]	27^	IO	MSB Data Bus signal
WEIM_DATA[3]	31^	IO	MSB Data Bus signal
WEIM_DATA[4]	70^	IO	MSB Data Bus signal
WEIM_DATA[5]	66^	IO	MSB Data Bus signal
WEIM_DATA[6]	58^	IO	MSB Data Bus signal
WEIM_DATA[7]	50^	IO	MSB Data Bus signal
WEIM_DATA[8]	52^	IO	MSB Data Bus signal
WEIM_DATA[9]	68	IO	MSB Data Bus signal
WEIM_DTACK_B	36	I	Data Acknowledge

Signal	Pin #	Type	Description
WEIM_EB_B[0]	24	O	Byte Enable signal
WEIM_EB_B[1]	76	O	Byte Enable signal
WEIM_LBA_B	25	O	Address Valid signal
WEIM_OE	17	O	Output Enable signal
WEIM_RW	8	O	Memory Write Enable signal
WEIM_WAIT	34	I	Ready/Busy/Wait signal

Note:

[^] Pins marked with ^ are being latched at boot to determine boot sequence. External drivers to this pin should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see Boot section.

5.19. Pulse Width Modulation (PWM)

The Pulse Width Modulation (PWM) has a 16-bit counter, and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit Resolution and a 4 x 16 data FIFO.

PWM Signals:

Signal	Pin #	Type	Description
PWM1_OUT	1*	O	PWM 1 Output
PWM1_OUT	105*	O	PWM 1 Output
PWM2_OUT	168	O	PWM 2 Output
PWM2_OUT	107*	O	PWM 2 Output
PWM3_OUT	181	O	PWM 3 Output
PWM3_OUT	187~	O	PWM 3 Output
PWM3_OUT	123*	O	PWM 3 Output
PWM4_OUT	170	O	PWM 4 Output
PWM4_OUT	185	O	PWM 4 Output
PWM4_OUT	125*	O	PWM 4 Output

Notes:

[*] Pins marked with * are connected to iMX7 SoC balls only on specific subsets of SOMs. Otherwise, ball is connected to On SOM devices and pin is used to export devices' interface.

[~] Pins marked with ~ are used by certain subsets of SOMs for internal SOM connections, Pin function must not be altered if using these subsets.

5.20. Keypad Port (KPP)

The Keypad Port (KPP) is a 16-bit peripheral that can be used as a keypad matrix Interface or as general purpose input/output (I/O).
The KPP provides interface for the keypad matrix with 2-point contact or 3-point contact keys. The KPP is designed to simplify the software task of scanning a keypad matrix. With appropriate software support, the KPP is capable of detecting, debouncing, and decoding one or multiple keys pressed simultaneously on the keypad

KPP Signals:

Signal	Pin #	Type	Description
KPP_COL[0]	19	IO	Column input or output pin 0
KPP_COL[0]	125*	IO	Column input or output pin 0
KPP_COL[1]	32	IO	Column input or output pin 1
KPP_COL[1]	117*	IO	Column input or output pin 1
KPP_COL[2]	12	IO	Column input or output pin 2
KPP_COL[2]	113*	IO	Column input or output pin 2
KPP_COL[3]	4	IO	Column input or output pin 3
KPP_COL[3]	107*	IO	Column input or output pin 3
KPP_COL[4]	189	IO	Column input or output pin 4
KPP_COL[4]	51*	IO	Column input or output pin 4
KPP_COL[5]	55*	IO	Column input or output pin 5
KPP_COL[6]	181	IO	Column input or output pin 6
KPP_COL[6]	67*	IO	Column input or output pin 7
KPP_COL[7]	77*	IO	Column input or output pin 7
KPP_COL[7]	174	IO	Column input or output pin 7
KPP_ROW[0]	21	IO	Row input or output pin 0
KPP_ROW[0]	123*	IO	Row input or output pin 0
KPP_ROW[1]	6	IO	Row input or output pin 1
KPP_ROW[1]	119*	IO	Row input or output pin 1
KPP_ROW[2]	14	IO	Row input or output pin 2
KPP_ROW[2]	111*	IO	Row input or output pin 2
KPP_ROW[3]	16	IO	Row input or output pin 3
KPP_ROW[3]	105*	IO	Row input or output pin 3
KPP_ROW[4]	49*	IO	Row input or output pin 4
KPP_ROW[5]	57*	IO	Row input or output pin 5
KPP_ROW[6]	185	IO	Row input or output pin 6
KPP_ROW[6]	69*	IO	Row input or output pin 6
KPP_ROW[7]	81*	IO	Row input or output pin 7
KPP_ROW[7]	178	IO	Row input or output pin 7

5.21. Flextimer (FTM)

The FlexTimer module (FTM) is a two-to-eight channel timer that supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The FTM time reference is a 16-bit counter that can be used as an unsigned or signed counter.

Signal	Pin #	Type	Description
FLEXTIMER1_CH[0]	55*	IO	FTM1 channel 0
FLEXTIMER1_CH[0]	118	IO	FTM1 channel 0
FLEXTIMER1_CH[1]	57*	IO	FTM1 channel 1
FLEXTIMER1_CH[1]	163	IO	FTM1 channel 1
FLEXTIMER1_CH[2]	63*	IO	FTM1 channel 2
FLEXTIMER1_CH[3]	61*	IO	FTM1 channel 3
FLEXTIMER1_CH[3]	128	IO	FTM1 channel 3
FLEXTIMER1_CH[4]	29^	IO	FTM1 channel 4
FLEXTIMER1_CH[5]	191	IO	FTM1 channel 5
FLEXTIMER1_CH[5]	38^	IO	FTM1 channel 5
FLEXTIMER1_CH[6]	33^	IO	FTM1 channel 6
FLEXTIMER1_CH[7]	189	IO	FTM1 channel 7
FLEXTIMER1_CH[7]	28^	IO	FTM1 channel 7
FLEXTIMER1_PHA	181	I	FTM1 Quadrature decoder phase A input
FLEXTIMER1_PHA	130	I	FTM1 Quadrature decoder phase A input
FLEXTIMER1_PHB	185	I	FTM1 Quadrature decoder phase B input
FLEXTIMER1_PHB	43~	I	FTM1 Quadrature decoder phase B input
FLEXTIMER2_CH[0]	77*	IO	FTM2 channel 0
FLEXTIMER2_CH[0]	122	IO	FTM2 channel 0
FLEXTIMER2_CH[1]	81*	IO	FTM2 channel 1
FLEXTIMER2_CH[1]	132	IO	FTM2 channel 1
FLEXTIMER2_CH[2]	83*	IO	FTM2 channel 2
FLEXTIMER2_CH[2]	126	IO	FTM2 channel 2
FLEXTIMER2_CH[3]	79*	IO	FTM2 channel 3
FLEXTIMER2_CH[3]	124	IO	FTM2 channel 3
FLEXTIMER2_CH[4]	30	IO	FTM2 channel 4
FLEXTIMER2_CH[4]	179	IO	FTM2 channel 4
FLEXTIMER2_CH[5]	22	IO	FTM2 channel 5
FLEXTIMER2_CH[5]	177	IO	FTM2 channel 5
FLEXTIMER2_CH[6]	20	IO	FTM2 channel 6
FLEXTIMER2_CH[6]	174	IO	FTM2 channel 6
FLEXTIMER2_CH[7]	26	IO	FTM2 channel 7
FLEXTIMER2_CH[7]	178	IO	FTM2 channel 7
FLEXTIMER2_PHA	74	I	FTM2 Quadrature decoder phase A input
FLEXTIMER2_PHA	172	I	FTM2 Quadrature decoder phase A input
FLEXTIMER2_PHB	76	I	FTM2 Quadrature decoder phase B input

Notes:

[*] Pins marked with * are connected to iMX7 SoC balls only on specific subsets of SOMs. Otherwise, ball is connected to On SOM devices and pin is used to export devices' interface.

[^] Pins marked with ^ are being latched at boot to determine boot sequence. External drivers to this pin should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see Boot section.

[~] Pins marked with ~ are used by certain subsets of SOMs for internal SOM connections, Pin function must not be altered if using these subsets.

5.22. Reference Clock Outputs/Inputs

The VAR-SOM-MX7-5G_V2 exposed 2 general purpose clock outputs (CLK01, CLKO2) for off chip peripherals and 4 external clock inputs controlled by the i.MX7 CCM module.
Please refer to the i.MX7 user manual regarding the configuration options for these clocks.

Signal	Pin #	Type	Description
CCM_CLKO1	118	O	Clock 1 Output
CCM_CLKO2	163	O	Clock 2 Output
CCM_EXT_CLK1	132	I	External Clock 1 Input
CCM_EXT_CLK2	126	I	External Clock 2 Input
CCM_EXT_CLK3	124	I	External Clock 3 Input
CCM_EXT_CLK4	130	I	External Clock 4 Input

5.23. General Purpose Input/Output (GPIO)

The GPIO general-purpose input/output peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.
When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register. In addition, the GPIO peripheral can produce CORE interrupts.

Signal	Pin #	Type	Description
GPIO1_IO[0]	170	IO	General Purpose Input Output Pin Bank 1 bit 0
GPIO1_IO[1]	1*	IO	General Purpose Input Output Pin Bank 1 bit 1
GPIO1_IO[2]	168	IO	General Purpose Input Output Pin Bank 1 bit 2
GPIO1_IO[3]	187~	IO	General Purpose Input Output Pin Bank 1 bit 3
GPIO1_IO[5]	191	IO	General Purpose Input Output Pin Bank 1 bit 5
GPIO1_IO[7]	189	IO	General Purpose Input Output Pin Bank 1 bit 7
GPIO1_IO[10]	181	IO	General Purpose Input Output Pin Bank 1 bit 10
GPIO1_IO[11]	185	IO	General Purpose Input Output Pin Bank 1 bit 11
GPIO1_IO[12]	183	IO	General Purpose Input Output Pin Bank 1 bit 12
GPIO1_IO[13]	120	IO	General Purpose Input Output Pin Bank 1 bit 13
GPIO2_IO[0]	16	IO	General Purpose Input Output Pin Bank 2 bit 0
GPIO2_IO[1]	4	IO	General Purpose Input Output Pin Bank 2 bit 1
GPIO2_IO[2]	14	IO	General Purpose Input Output Pin Bank 2 bit 2
GPIO2_IO[3]	12	IO	General Purpose Input Output Pin Bank 2 bit 3
GPIO2_IO[4]	6	IO	General Purpose Input Output Pin Bank 2 bit 4
GPIO2_IO[5]	32	IO	General Purpose Input Output Pin Bank 2 bit 5
GPIO2_IO[6]	21	IO	General Purpose Input Output Pin Bank 2 bit 6
GPIO2_IO[7]	19	IO	General Purpose Input Output Pin Bank 2 bit 7
GPIO2_IO[8]	17	IO	General Purpose Input Output Pin Bank 2 bit 8
GPIO2_IO[9]	8	IO	General Purpose Input Output Pin Bank 2 bit 9
GPIO2_IO[10]	2	IO	General Purpose Input Output Pin Bank 2 bit 10
GPIO2_IO[11]	18	IO	General Purpose Input Output Pin Bank 2 bit 11
GPIO2_IO[12]	25	IO	General Purpose Input Output Pin Bank 2 bit 12
GPIO2_IO[13]	34	IO	General Purpose Input Output Pin Bank 2 bit 13
GPIO2_IO[14]	24	IO	General Purpose Input Output Pin Bank 2 bit 14
GPIO2_IO[15]	10	IO	General Purpose Input Output Pin Bank 2 bit 15
GPIO2_IO[16]	49*	IO	General Purpose Input Output Pin Bank 2 bit 16
GPIO2_IO[17]	51*	IO	General Purpose Input Output Pin Bank 2 bit 17
GPIO2_IO[18]	55*	IO	General Purpose Input Output Pin Bank 2 bit 18
GPIO2_IO[19]	57*	IO	General Purpose Input Output Pin Bank 2 bit 19
GPIO2_IO[20]	63*	IO	General Purpose Input Output Pin Bank 2 bit 20
GPIO2_IO[21]	61*	IO	General Purpose Input Output Pin Bank 2 bit 21
GPIO2_IO[22]	67*	IO	General Purpose Input Output Pin Bank 2 bit 22
GPIO2_IO[23]	69*	IO	General Purpose Input Output Pin Bank 2 bit 23
GPIO2_IO[24]	77*	IO	General Purpose Input Output Pin Bank 2 bit 24
GPIO2_IO[25]	81*	IO	General Purpose Input Output Pin Bank 2 bit 25
GPIO2_IO[26]	83*	IO	General Purpose Input Output Pin Bank 2 bit 26
GPIO2_IO[27]	79*	IO	General Purpose Input Output Pin Bank 2 bit 27
GPIO2_IO[28]	73	IO	General Purpose Input Output Pin Bank 2 bit 28
GPIO2_IO[29]	75	IO	General Purpose Input Output Pin Bank 2 bit 28
GPIO2_IO[30]	74	IO	General Purpose Input Output Pin Bank 2 bit 30

Signal	Pin #	Type	Description
GPIO2_IO[31]	76	IO	General Purpose Input Output Pin Bank 2 bit 31
GPIO3_IO[0]	48	IO	General Purpose Input Output Pin Bank 3 bit 0
GPIO3_IO[1]	42	IO	General Purpose Input Output Pin Bank 3 bit 1
GPIO3_IO[2]	44	IO	General Purpose Input Output Pin Bank 3 bit 2
GPIO3_IO[3]	46	IO	General Purpose Input Output Pin Bank 3 bit 3
GPIO3_IO[4]	36	IO	General Purpose Input Output Pin Bank 3 bit 4
GPIO3_IO[5]	40^	IO	General Purpose Input Output Pin Bank 3 bit 5
GPIO3_IO[6]	23^	IO	General Purpose Input Output Pin Bank 3 bit 6
GPIO3_IO[7]	27^	IO	General Purpose Input Output Pin Bank 3 bit 7
GPIO3_IO[8]	31^	IO	General Purpose Input Output Pin Bank 3 bit 8
GPIO3_IO[9]	70^	IO	General Purpose Input Output Pin Bank 3 bit 9
GPIO3_IO[10]	66^	IO	General Purpose Input Output Pin Bank 3 bit 10
GPIO3_IO[11]	58^	IO	General Purpose Input Output Pin Bank 3 bit 11
GPIO3_IO[12]	50^	IO	General Purpose Input Output Pin Bank 3 bit 12
GPIO3_IO[13]	52^	IO	General Purpose Input Output Pin Bank 3 bit 13
GPIO3_IO[14]	68^	IO	General Purpose Input Output Pin Bank 3 bit 14
GPIO3_IO[15]	64^	IO	General Purpose Input Output Pin Bank 3 bit 15
GPIO3_IO[16]	54^	IO	General Purpose Input Output Pin Bank 3 bit 16
GPIO3_IO[17]	56^	IO	General Purpose Input Output Pin Bank 3 bit 17
GPIO3_IO[18]	62^	IO	General Purpose Input Output Pin Bank 3 bit 18
GPIO3_IO[19]	72^	IO	General Purpose Input Output Pin Bank 3 bit 19
GPIO3_IO[20]	60^	IO	General Purpose Input Output Pin Bank 3 bit 20
GPIO3_IO[21]	29^	IO	General Purpose Input Output Pin Bank 3 bit 21
GPIO3_IO[22]	38^	IO	General Purpose Input Output Pin Bank 3 bit 22
GPIO3_IO[23]	33^	IO	General Purpose Input Output Pin Bank 3 bit 23
GPIO3_IO[24]	28^	IO	General Purpose Input Output Pin Bank 3 bit 24
GPIO3_IO[25]	30	IO	General Purpose Input Output Pin Bank 3 bit 25
GPIO3_IO[26]	22	IO	General Purpose Input Output Pin Bank 3 bit 26
GPIO3_IO[27]	20	IO	General Purpose Input Output Pin Bank 3 bit 27
GPIO3_IO[28]	26	IO	General Purpose Input Output Pin Bank 3 bit 28
GPIO4_IO[0]	159	IO	General Purpose Input Output Pin Bank 4 bit 0
GPIO4_IO[1]	161	IO	General Purpose Input Output Pin Bank 4 bit 1
GPIO4_IO[4]	156	IO	General Purpose Input Output Pin Bank 4 bit 4
GPIO4_IO[5]	158	IO	General Purpose Input Output Pin Bank 4 bit 5
GPIO4_IO[6]	152	IO	General Purpose Input Output Pin Bank 4 bit 6
GPIO4_IO[7]	154	IO	General Purpose Input Output Pin Bank 4 bit 7
GPIO4_IO[10]	169~	IO	General Purpose Input Output Pin Bank 4 bit 10
GPIO4_IO[11]	171~	IO	General Purpose Input Output Pin Bank 4 bit 11
GPIO4_IO[12]	157	IO	General Purpose Input Output Pin Bank 4 bit 12
GPIO4_IO[13]	155	IO	General Purpose Input Output Pin Bank 4 bit 13
GPIO4_IO[14]	175	IO	General Purpose Input Output Pin Bank 4 bit 14
GPIO4_IO[15]	173	IO	General Purpose Input Output Pin Bank 4 bit 15
GPIO4_IO[20]	153	IO	General Purpose Input Output Pin Bank 4 bit 20
GPIO4_IO[21]	149	IO	General Purpose Input Output Pin Bank 4 bit 21
GPIO4_IO[22]	147	IO	General Purpose Input Output Pin Bank 4 bit 22
GPIO4_IO[23]	151	IO	General Purpose Input Output Pin Bank 4 bit 23
GPIO5_IO[0]	118	IO	General Purpose Input Output Pin Bank 5 bit 0
GPIO5_IO[1]	163	IO	General Purpose Input Output Pin Bank 5 bit 1
GPIO5_IO[3]	128	IO	General Purpose Input Output Pin Bank 5 bit 3
GPIO5_IO[4]	122	IO	General Purpose Input Output Pin Bank 5 bit 4
GPIO5_IO[5]	132	IO	General Purpose Input Output Pin Bank 5 bit 5
GPIO5_IO[6]	126	IO	General Purpose Input Output Pin Bank 5 bit 6
GPIO5_IO[7]	124	IO	General Purpose Input Output Pin Bank 5 bit 7
GPIO5_IO[8]	130	IO	General Purpose Input Output Pin Bank 5 bit 8
GPIO5_IO[9]	43~	IO	General Purpose Input Output Pin Bank 5 bit 9
GPIO5_IO[10]	45~	IO	General Purpose Input Output Pin Bank 5 bit 10
GPIO6_IO[16]	176	IO	General Purpose Input Output Pin Bank 6 bit 16
GPIO6_IO[17]	172	IO	General Purpose Input Output Pin Bank 6 bit 17
GPIO6_IO[19]	179	IO	General Purpose Input Output Pin Bank 6 bit 19
GPIO6_IO[20]	177	IO	General Purpose Input Output Pin Bank 6 bit 20
GPIO6_IO[21]	174	IO	General Purpose Input Output Pin Bank 6 bit 21
GPIO6_IO[22]	178	IO	General Purpose Input Output Pin Bank 6 bit 22

Signal	Pin #	Type	Description
GPIO7_IO[0]	105*	IO	General Purpose Input Output Pin Bank 7 bit 0
GPIO7_IO[1]	107*	IO	General Purpose Input Output Pin Bank 7 bit 1
GPIO7_IO[2]	111*	IO	General Purpose Input Output Pin Bank 7 bit 2
GPIO7_IO[3]	113*	IO	General Purpose Input Output Pin Bank 7 bit 3
GPIO7_IO[4]	119*	IO	General Purpose Input Output Pin Bank 7 bit 4
GPIO7_IO[5]	117*	IO	General Purpose Input Output Pin Bank 7 bit 5
GPIO7_IO[6]	123*	IO	General Purpose Input Output Pin Bank 7 bit 6
GPIO7_IO[7]	125*	IO	General Purpose Input Output Pin Bank 7 bit 7
GPIO7_IO[8]	129*	IO	General Purpose Input Output Pin Bank 7 bit 8
GPIO7_IO[9]	133*	IO	General Purpose Input Output Pin Bank 7 bit 9
GPIO7_IO[10]	135*	IO	General Purpose Input Output Pin Bank 7 bit 10
GPIO7_IO[11]	131*	IO	General Purpose Input Output Pin Bank 7 bit 11
GPIO7_IO[12]	9*	IO	General Purpose Input Output Pin Bank 7 bit 12
GPIO7_IO[13]	13*	IO	General Purpose Input Output Pin Bank 7 bit 13
GPIO7_IO[14]	7*	IO	General Purpose Input Output Pin Bank 7 bit 14
GPIO7_IO[15]	15*	IO	General Purpose Input Output Pin Bank 7 bit 15

Notes:

[*] Pins marked with * are connected to iMX7 SoC balls only on specific subsets of SOMs. Otherwise, ball is connected to On SOM devices and pin is used to export devices' interface.

[^] Pins marked with ^ are being latched at boot to determine boot sequence. External drivers to this pin should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see Boot section.

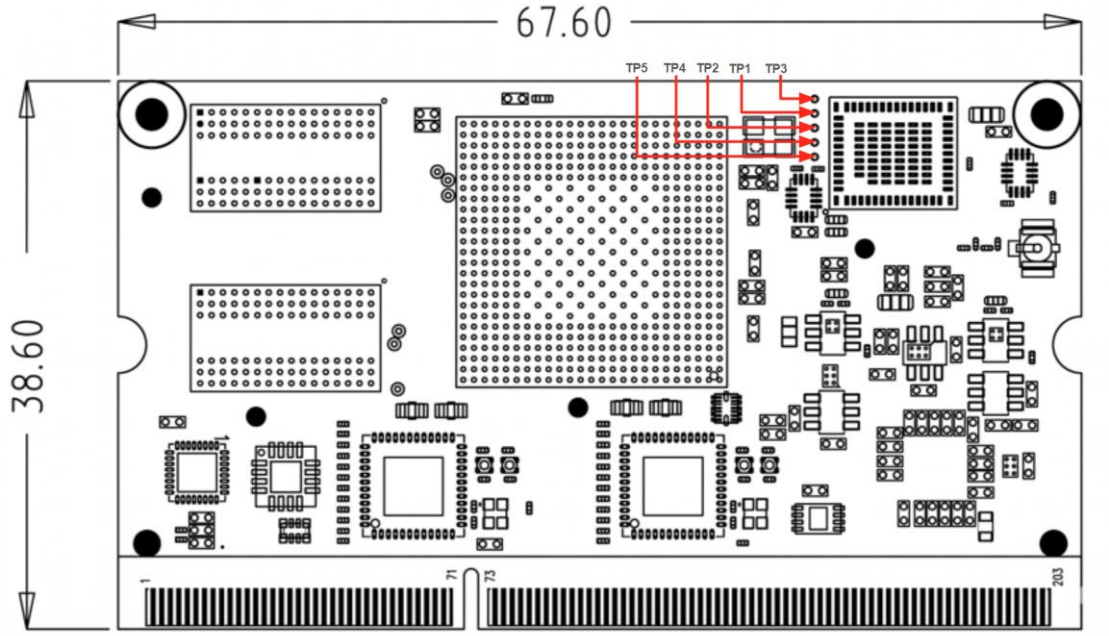
[~] Pins marked with ~ are used by certain subsets of SOMs for internal SOM connections, Pin function must not be altered if using these subsets.

5.24. JTAG

The System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals. The JTAG Interface is exported through Test Points.

JTAG signals Test Points:

Signal	TP #	Type	Description
JTAG_TMS	1	I	JTAG test mode select
JTAG_TDI	2	I	JTAG data-in
JTAG_TDO	3	O	JTAG data-out
JTAG_TCK	4	O	JTAG test clock
JTAG_RST_B	5	I	JTAG reset



5.25. General System Control

5.25.1. Boot configuration

The VAR-SOM-MX7-5G_V2 can be programmed to boot from the following sources:

- On board NAND Flash memory (if available)
- On board eMMC Flash memory (if available)
- External SD Card

The selection of the boot mode is done via strap options resistors on BT_CFG lines. Attention should be paid using these boot strap pins as inputs to the SOM. External drivers should be disabled in time of Reset otherwise they may change the boot option and the SOM will not boot.

Signal	Pin #	Description	NAND	eMMC	SD Card
LCD_DATA[0]	40	BT_CFG[0]	0	0	0
LCD_DATA[1]	23	BT_CFG[1]	0	0	0
LCD_DATA[2]	27	BT_CFG[2]	0	0	0
LCD_DATA[3]	31	BT_CFG[3]	0	0	0
CSI1_VSYNC	70	BT_CFG[4]	0	0	0
CSI1_HSYNC	66	BT_CFG[5]	0	0	0
CSI1_PIXCLK	58	BT_CFG[6]	0	0	0
CSI1_MCLK	50	BT_CFG[7]	0	0	0
CSI1_DATA[9]	52	BT_CFG[8]	0	0	0
CSI1_DATA[8]	68	BT_CFG[9]	0	0	0
CSI1_DATA[7]	64	BT_CFG[10]	1	0	0
CSI1_DATA[6]	54	BT_CFG[11]	0	1	0
CSI1_DATA[5]	56	BT_CFG[12]	1	0	1
CSI1_DATA[4]	62	BT_CFG[13]	1	1	0
CSI1_DATA[3]	72	BT_CFG[14]	0	0	0
CSI1_DATA[2]	60	BT_CFG[15]	0	0	0
LCD_DATA[16]	29	BT_CFG[16]	0	0	0
LCD_DATA[17]	38	BT_CFG[17]	0	0	0
LCD_DATA[18]	33	BT_CFG[18]	0	0	0
LCD_DATA[19]	28	BT_CFG[19]	0	0	0

Note: 0 – Represents pull down or floating. 1 – Represents pull up of 10KΩ or stronger.

5.25.2. General System Control Signals

Signal	Pin #	Type	Description
POR_B	160	I O	iMX7 SoC Power On Reset Input signal, PMIC Reset open drain output signal '0' logic will reset the system
PMIC_PWRON	162	I	PMIC Power On signal
PMIC_STBY_REQ	164	O	iMX7 SoC Standby request output
MX7_ONOFF	148	I	iMX7 SoC ONOFF Signal

Note: A delay should be added on PMIC_PWRON signal, see reference schematics.

5.26. Power

5.26.1. Power

Signal	Pin #	Type	Description
VCC_3V3_IN	137,138,139, 140,141,142, 143,144,145, 146	Power	VAR-SOM-MX7-5G_V2 Single 3.3V Supply voltage input
USB_HOST_VBUS	102	Power	USB HOST VBUS (5V) input
USB_OTG_VBUS	110	Power	USB OTG VBUS (5V) input
VCC_3V3	134	Power	SOM Peripherals 3.3V Output
LICELL	136	Power	3.0V RTC back-up battery supply input
VSNVS	150	Power	RTC Domain 3.0V power rail Output

5.26.2. Ground

Signal	Pin #	Type	Description
GND	47,53,59,65 71,78,84,85 90,91,96,97, 103,109,115, 116,121,127, 180,186,192 193,198,203, 204	Power	Digital ground
AGND	5,11	Power	Audio Interface Ground Reference

6. Electrical specifications

6.1. Absolute maximum ratings

Parameter		Min	Max	Unit
VCC_3V3_IN	Main supply input voltage	-0.3	3.6	V
LICELL	3.0V RTC back-up battery supply input	-0.3	3.6	V
USB_VBUS	USB_HOST_VBUS, USB_OTG_VBUS	-0.3	5.25	V

6.2. Operating conditions

Parameter		Min	Typ	Max	Unit
VCC_3V3_IN	Main supply input voltage	3.15	3.3	3.45	V
LICELL	3.0V RTC back-up battery supply input	1.8	3.0	3.3	V
USB_VBUS	USB_HOST_VBUS, USB_OTG_VBUS	4.75	5.0	5.25	V

6.3. Power Consumption

VAR-SOM-MX7-5G_V2:

Mode	Voltage	Current	Power	Notes
Run	3.3V	218mA	719.4mW	Linux up, Wi-Fi connected and Iperf is running 802.11 ac 5GHz
Run	3.3V	168mA	544.4mW	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz
Run	3.3V	140mA	462mW	Linux up
Standby	3.3V	TBD	TBD	Memory retention mode
Off (RTC)	3.0V	0.65mA	1.95mW	All power rails are Off, only Internal SoC RTC is powered

Note: The SOM which includes an onboard Wi-Fi module generates short-duration current spikes during initialization, RF calibration, and wireless transmission. The carrier board should provide a 3.3V power supply capable of delivering at least 2 A, with adequate transient response and low output impedance.

NOTE

Setup:
HW:

VAR-SOM-MX7-5G_V2_1024R_8N_AC_EC1_EC2_TP_WBD_IT_REV2.0

SW: mx7-yocto-scarthgap-6.6.y_2.2.2-v1.0

DISCLAIMER:

The power consumption measurements apply only to limited operation scenarios. Actual power consumption may vary depending on the interfacing peripherals and user application modes; Users must conduct testing per their specific operation scenarios.

Depending on the specific use cases and end product system design, an appropriate thermal solution should be applied.

7. Environmental Specifications

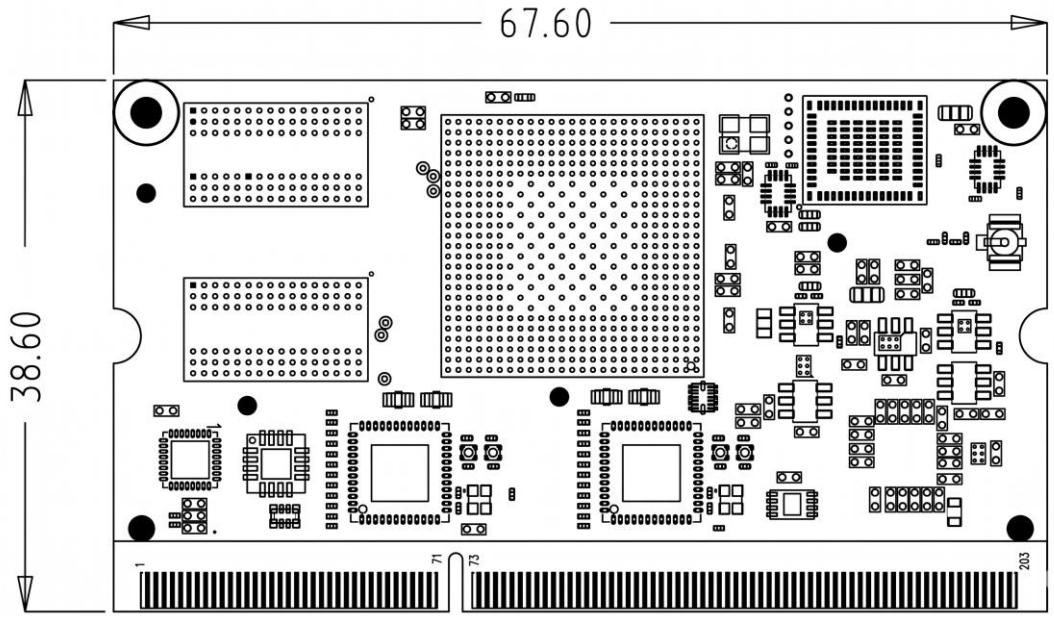
	Min	Max
Commercial Operating Temperature Range	0 ^{0}C	+70 ^{0}C
Extended Operating Temperature Range	-20	+85 ^{0}C
Referring MIL-HDBK-217F-2 Parts Count Reliability Prediction Method Model:		
25Deg Celsius, Class B-1, GM	121 Khrs >	
25Deg Celsius, Class B-1, GB	1400 Khrs >	
Storage temperature	-40°C	85°C
Relative humidity (operation)	10%	90%
Relative humidity (storage)	05%	95%

Note: Extended and Industrial Temperature is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

8. Mechanical Drawings

Top View [mm]

VAR-SOM-MX7-5G_V2:



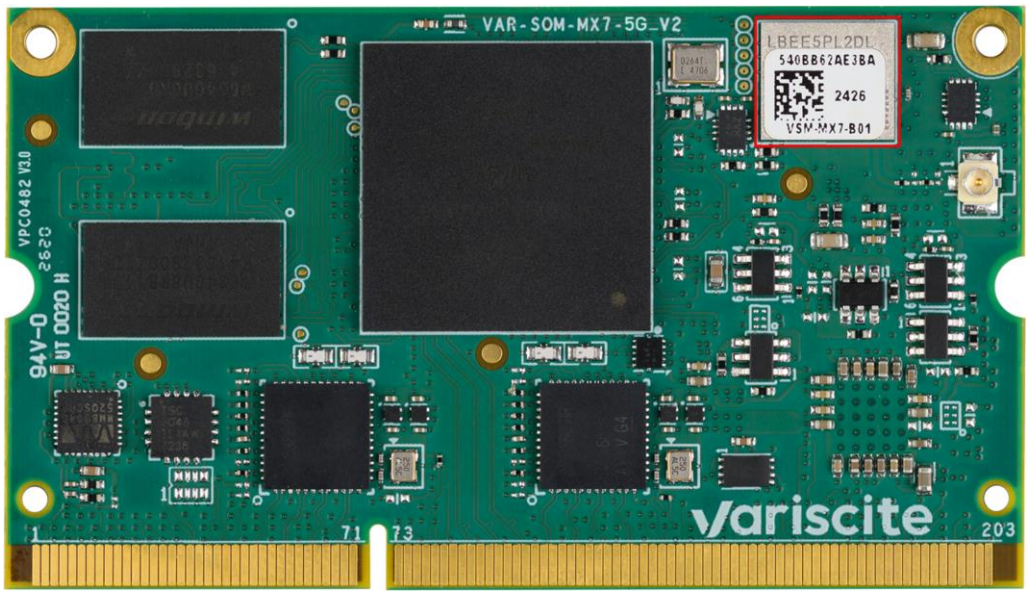
CAD files are available for download at http://www.variscite.com/

Note:

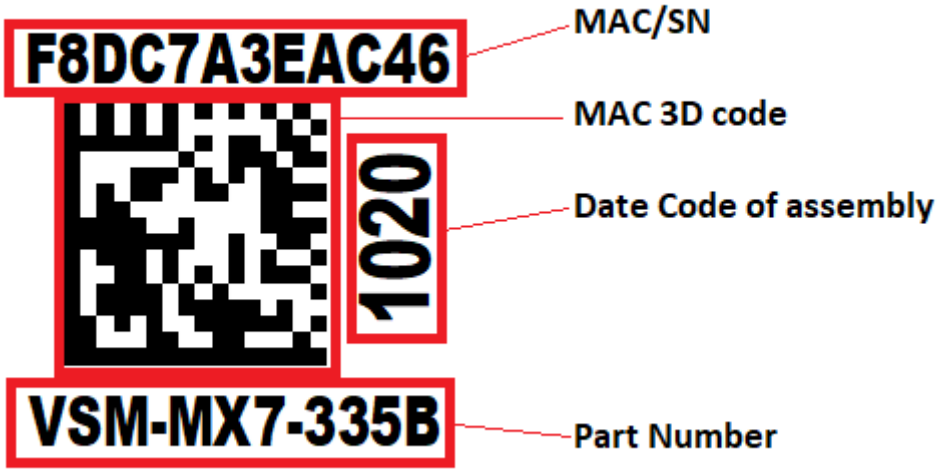
2 SMT type screw-in standoff is recommended for robust fastening of the SOM to the Carrier board.
Suggested P/N is Penn Engineering SMTSO-M2-3-ET
Recommended torque for tightening the screws is ~1lb/in (~0.113N/m).

9. Sticker

A sticker with manufacturing details is added in time of assembly process.
Sticker location:



Sticker information example:



10. Legal Notice

Variscite Ltd. ("Variscite") products and services are sold subject to Variscite terms and conditions of sale, delivery and payment supplied at the time of order acknowledgement.

Variscite warrants performance of its products to the specifications in effect at the date of shipment. Variscite reserves the right to make changes to its products and specifications or to discontinue any product or service without notice. Customers should therefore obtain the latest version of relevant product information from Variscite to verify that their reference is current.

Testing and other quality control techniques are utilized to the extent that Variscite deems necessary to support its warranty.

Specific testing of all parameters of each device is not necessarily performed unless required by law or regulation.

In order to minimize risks associated with customer applications, the customer must use adequate design and operating safeguards to minimize inherent or procedural hazards. Variscite is not liable for applications assistance or customer product design. The customer is solely responsible for its selection and use of Variscite products. Variscite is not liable for such selection or use or for use of any circuitry other than circuitry entirely embodied in a Variscite product.

Variscite products are not intended for use in life support systems, appliances, nuclear systems or systems where malfunction can reasonably be expected to result in personal injury, death or severe property or environmental damage. Any use of products by the customer for such purposes is at the customer's own risk.

Variscite does not grant any license (express or implied) under any patent right, copyright, mask work right or other intellectual property right of Variscite covering or relating to any combination, machine, or process in which its products or services might be or are used. Any provision or publication of any third party's products or services does not constitute Variscite's approval, license, warranty or endorsement thereof. Any third party trademarks contained in this document belong to the respective third party owner.

Reproduction of information from Variscite datasheets is permissible only if reproduction is without alteration and is accompanied by all associated copyright, proprietary and other notices (including this notice) and conditions. Variscite is not liable for any un-authorized alteration of such information or for any reliance placed thereon.

Any representations made, warranties given, and/or liabilities accepted by any person which differ from those contained in this datasheet or in Variscite's standard terms and conditions of sale, delivery and payment are made, given and/or accepted at that person's own risk. Variscite is not liable for any such representations, warranties or liabilities or for any reliance placed thereon by any person.

11. Warranty Terms

Variscite guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and Variscite's sole liability shall be for Variscite, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

Disclaimer of Warranty

THIS WARRANTY IS MADE IN LIEU OF ANY OTHER WARRANTY, WHETHER EXPRESSED, OR IMPLIED, OF MERCHANTABILITY, FITNESS FOR A SPECIFIC PURPOSE, NON-INFRINGEMENT OR THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION, EXCEPT THE WARRANTY EXPRESSLY STATED HEREIN. THE REMEDIES SET FORTH HEREIN SHALL BE THE SOLE AND EXCLUSIVE REMEDIES OF ANY PURCHASER WITH RESPECT TO ANY DEFECTIVE PRODUCT.

Limitation on Liability

UNDER NO CIRCUMSTANCES SHALL VARISCITE BE LIABLE FOR ANY LOSS, DAMAGE OR EXPENSE SUFFERED OR INCURRED WITH RESPECT TO ANY DEFECTIVE PRODUCT. IN NO EVENT SHALL VARISCITE BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES THAT YOU MAY SUFFER DIRECTLY OR INDIRECTLY FROM USE OF ANY PRODUCT. BY ORDERING THE SOM, THE CUSTOMER APPROVES THAT THE VARISCITE SOM, HARDWARE AND SOFTWARE, WAS THOROUGHLY TESTED AND HAS MET THE CUSTOMER'S REQUIREMETS AND SPECIFICATIONS.

12. Contact Information

Headquarters:
Variscite Ltd.

9, Hamelacha Street
Lod
P.O.B 1121
Airport City, 70100
ISRAEL

Tel: +972 (9) 9562910
Fax: +972 (9) 9589477

Sales: sales@variscite.com
Technical Support: support@variscite.com

Corporate Website: variscite.com